The Alta

Hardware Reference Manual

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Preface

Chapter P

P.1 Purpose

This Hardware Reference Manual is intended for anyone using the Alta analog frame grabber. The purpose of this manual is two-fold. First, this manual completely describes how the board works. Second, it is a reference manual describing in detail the functionality of all of the board's registers.

P.1.1 Support Services

BitFlow, Inc. provides both sales and technical support for the Alta family of products.

P.1.2 Technical Support

Our web site is www.bitflow.com.

Technical support is available at 781-932-2900 from 9:00 AM to 6:00 PM Eastern Standard Time, Monday through Friday.

For technical support by email (support@bitflow.com) or by FAX (781-933-9965), please include the following:

Product name
Camera type and mode being used
Software revision number
Computer CPU type, PCI chipset, bus speed
Operating system
Example code (if applicable)

P.1.3 Sales Support

Contact your local BitFlow Sales Representative, Dealer, or Distributor for information about how BitFlow can help you solve your most demanding camera interfacing problems. Refer to the BitFlow, Inc. web site (www.bitflow.com) for a list of North American representatives and worldwide distributors.

P.1.4 Conventions

Table P-1 shows the conventions that are used for numerical notation in this manual.

Table P-1 Base Abbreviations

Base	Designator	Example
Binary	b	1010b
Decimal	None	4223
Hexidecimal	h	12fah

Table P-2 shows the numerical abbreviations that are used in this manual.

Table P-2 Numeric Abbreviations

Abbreviation	Value	Example
K	1024	256K
M	1048576	1M

General Description and Architecture

Chapter 1

1.1 The Alta family

The purpose of this chapter is to explain, at a block diagram level, how the Alta analog frame grabber works, and what different versions are available. There are three main models in the Alta family:

ALT-PCE-AN1, supports one analog camera
ALT-PCE-AN2, supports one to two independent analog cameras
ALT-PCE-AN4, supports one to four independent analog cameras

The differences between the models are explained in more detail in Section 1.5.

1.1.1 Virtual vs. Hardware

It's important to understand how this manual works. Some chapters of this manual discuss the Alta as a hardware platform (this chapter is a good example). While other chapters discuss the details of the virtual frame grabbers (VFG) that this hardware platform supports. The concept of the virtual frame grabber is described below, but basically the idea is that one hardware platform can support more than one device. In the case of the Alta, these devices are frame grabbers.

Note that we are not using the word virtual here in the sense of "a software virtualization of a hardware device", these VFGs are real hardware. The reason we using "virtual" is because the term "frame grabber" has more than one meaning. It can mean the piece of hardware that you put in your computer, or it can mean the device that the your software application is controlling and getting images from. For the purposes of this manual, "virtual frame grabber" means the device that your application is interfacing to. While this might sound complicated, the implementation is simple. You plug our Alta frame grabber into your PC, and your application interacts with one or more VFGs available. Everything else is taken care of by the BitFlow drivers.

1.1.2 The Virtual Frame Grabber (VFG)

The Alta is another BitFlow frame grabber family that supports the concept of the virtual frame grabber (VFG). The Karbon-CL is another family that works in a similar way. The idea behind the VFG is to separate the hardware platform (connectors, laminate, FPGAs, etc.) from the frame grabbing functionality that software applications work with. The primary reason behind this separation is that the turn around time for hardware is much longer than the turn around time for modifying virtual frame grabbers. To create a brand new virtual frame grabber, or to modify an existing one, simply requires writing new firmware or updating existing firmware.

The idea of modifying a frame grabber by making changes to its firmware is not new. BitFlow has been doing this since its very first product. However, what is important about VFG based boards, is the fact the entire frame grabber is written in firmware. The only fixed hardware components are the interfaces to the outside world (e.g. the CL chips on the front end). Everything else that makes up the board, camera control, data buffering, DMA engine, etc. is written in firmware. This gives the VFG platform incredible levels of flexibility and opens the door to unlimited customization.

To understand which models support which modes see Section 1.5. Also to see examples of the different modes, see Section 1.3. However, keep in mind, the Alta is only limited by your imagination, if you need a mode you don't see, just let us know.

1.1.3 Alta PCI Configuration Spaces

The three basic Alta models support from one to four VFGs. Each VFG has its own configuration space (PCI interface) and will look like a separate device to the operating system. Each VFG will be connected to one Analog Front End (AFE) interface chip. Each AFE has a powerful set of features described later in this chapter. Figure 1-1 shows the block diagram of the AN1 model1. The AN1 models support one analog camera. Figure 1-2 shows the diagram of the AN2 model, which support two analog cameras, and Figure 1-3 shows the diagram of the AN4 model, which supports 4 analog cameras.

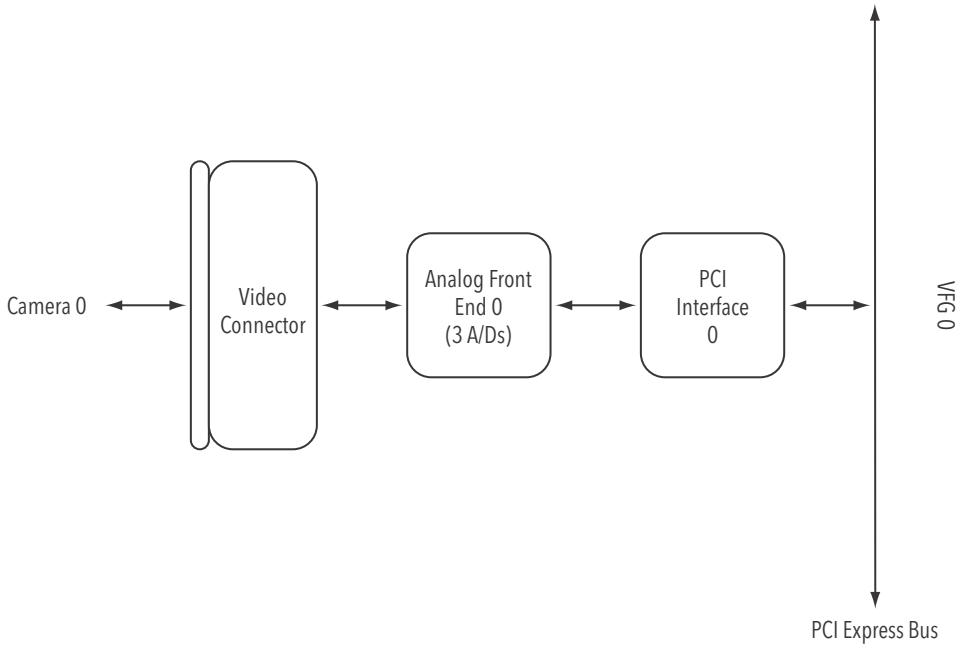

Figure 1-1 ALT-PCE-AN1 Block Diagram

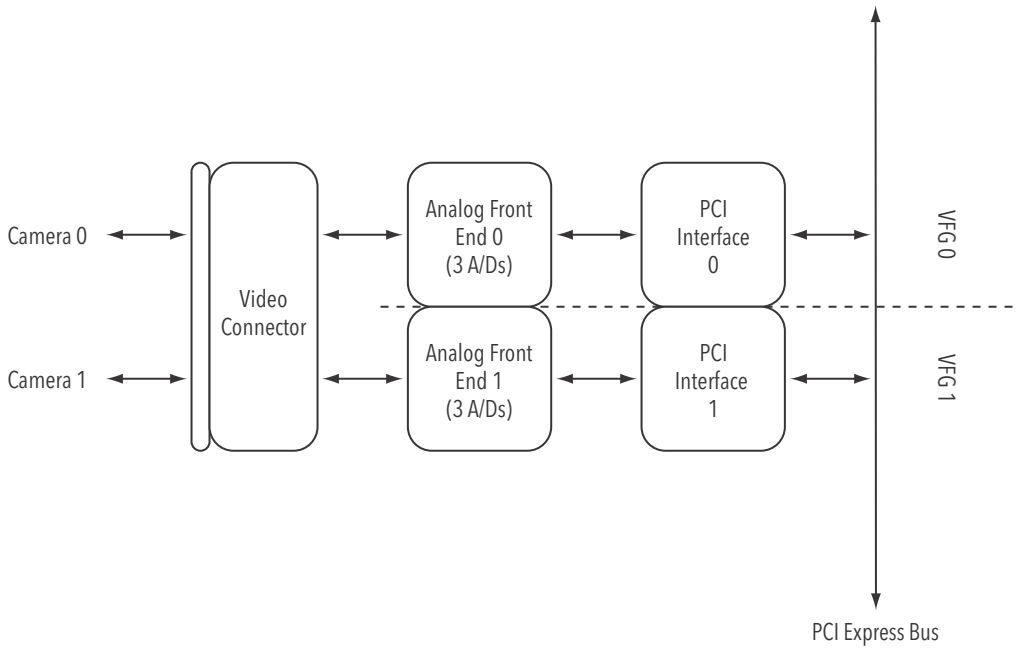

Figure 1-2 ALT-PCE-AN2 Block Diagram

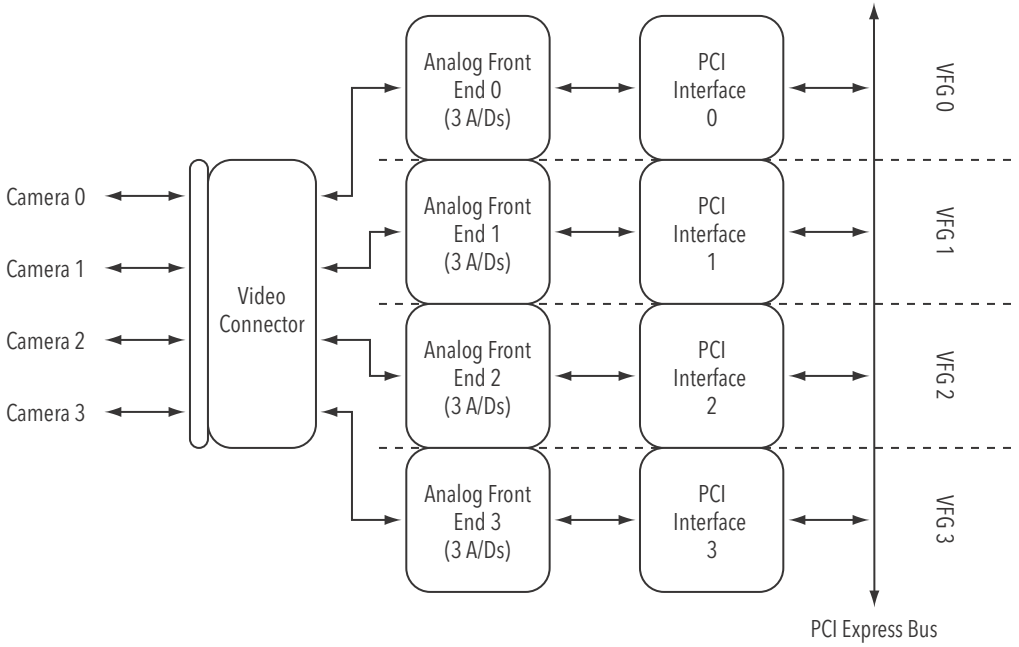

Figure 1-3 ALT-PCE-AN4 Block Diagram

1.2 Firmware, Camera Files and Downloads

Note that all the devices present on an Alta will appear in SysReg as separate BitFlow Boards Found. The order that the VFGs appear in SysReg is determined by the operating system and is somewhat arbitrary. However, SysReg lists the connector(s) associated with each VFG, so that the connection can be made between VFG and physical connected camera.

Recall that, even though Alta may appear like four frame grabbers, there is only one actual hardware platform. For this reason the firmware of the VFGs on one board are linked. The selection of the master VFG, determines the configurations of all of the slave VFGs. For example, if you have a ALT-PCE-AN4 and you configured the master VFG with a two-tap camera, then the slave VFG will also have to be configure for a two-tap camera. In all other ways, however, the two configurations do not have to match. If you have a requirement where this rule must be broken, please contact BitFlow's support department. Custom combinations of firmware are available.

If there is a mismatch between the firmware required by one VFG's camera file and the firmware required by another VFG's camera file, the master VFG's firmware will get priority. In practice this means that if you change the camera file for the master VFG, and it requires different firmware than is already on the board, new firmware will be downloaded next time you start an application. However, in the case of a slave VFG, if different firmware is required than is on the board, an error message will pop up indicating the problem. Thus all the camera files for a all the VFGs on one Alta should all require the same firmware. That said, if you have a custom need for a particular arrangement of cameras, please let us know. We can create custom firmware to solve almost any problem.

1.3 General Description

The Alta is a x4 PCI Express board. It can work in any PCI Express slot that it can fit it. Usually this means an x4, x8 or x16 slot. However, some mother boards have x1 slots with x4 connectors. The Alta will work in these slots, although performance my be somewhat reduced.

Figure 1-4 shows the block diagram of the Alta hardware platform. Although this block diagram looks like a single device, the firmware inside the main control block can be up to four virtual frame grabbers (VFGs). The number of VFGs depends on the Alta model. Subsequent sections discussed the details of the various blocks.

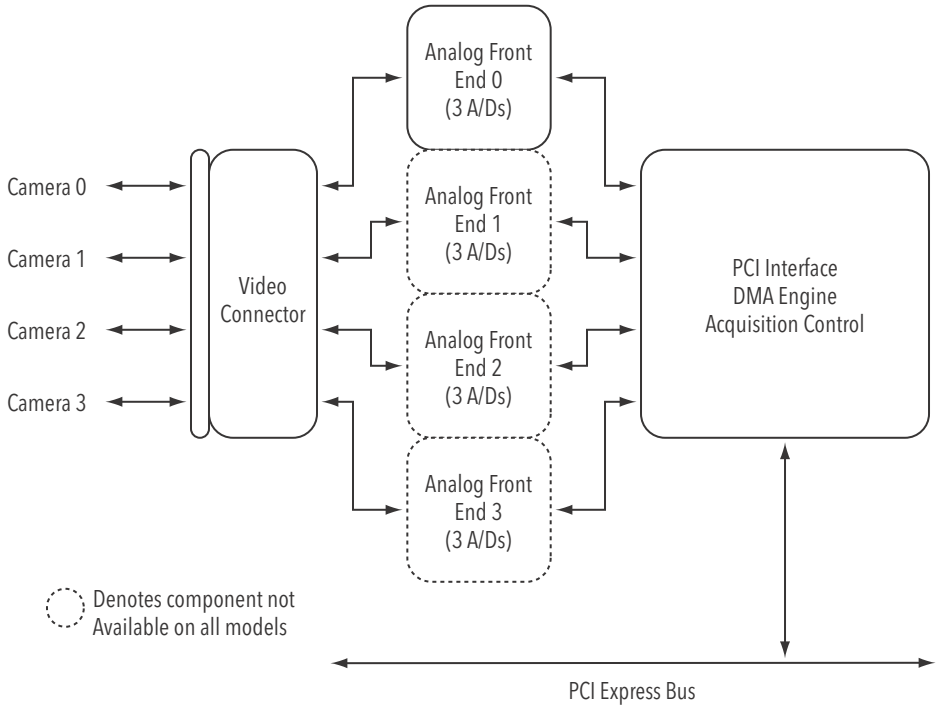

Figure 1-4 Alta Hardware Platform

1.4 The Analog Virtual Frame Grabber (Analog VGF)

Figure 1-5 illustrates the complete analog VFG use on the Alta. Keep in the mind that the ALT-PCE-AN4 model has four independent copies of this analog VFG, and the ALT-PCE-AN2 has two independent analog VFGs. Independent means that they each can be programmed completely differently for different cameras, they do not have to be synchronize, they are in all ways like completely separate frame grabbers.

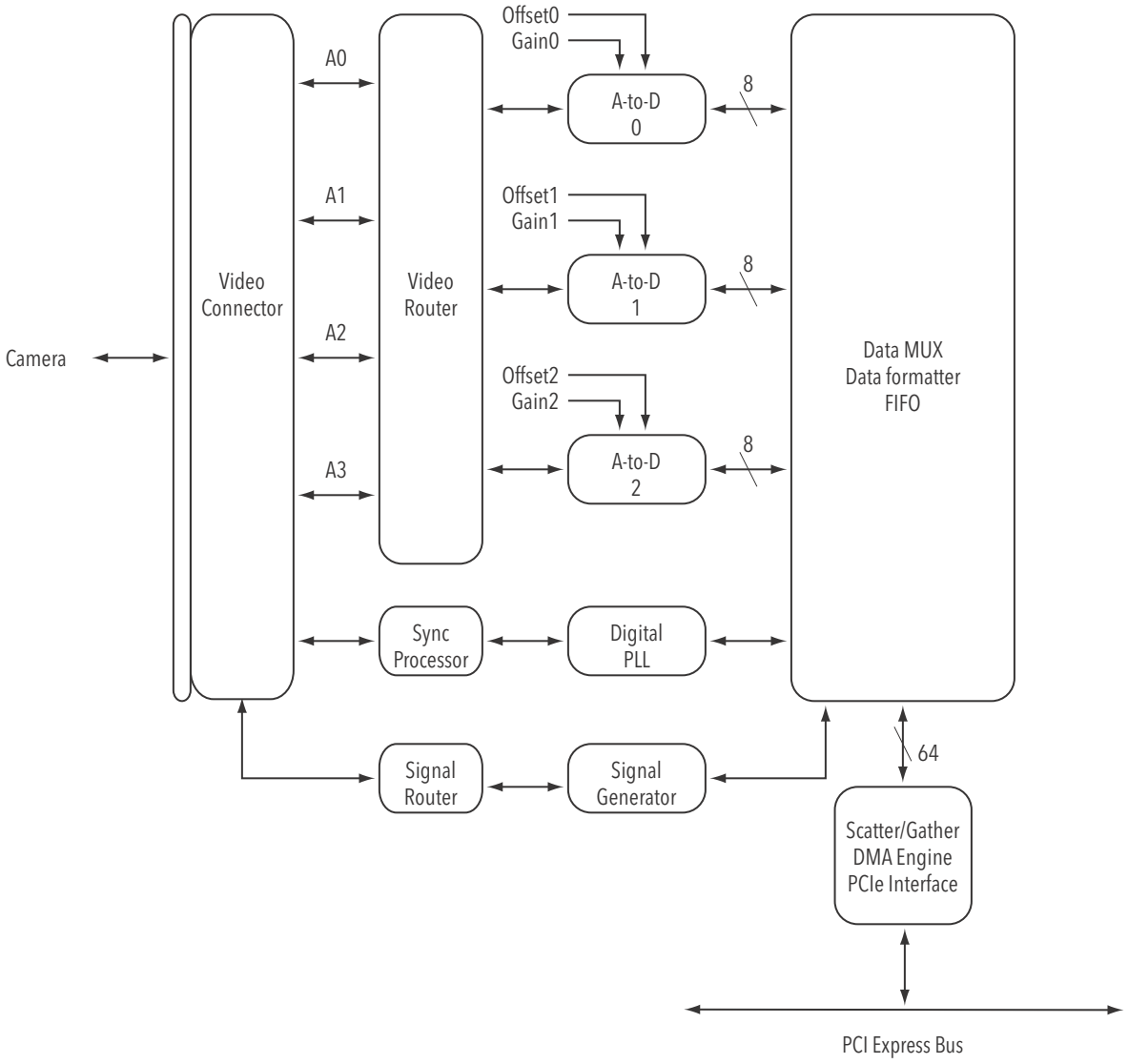

Figure 1-5 Complete Analog VFG

Each VFG is divided into two main sections, the analog front end (AFE) and the digital data handling circuitry. The AFE is responsible for pre-conditioning the incoming analog signal(s), analog to digital convention, creating the pixel clock from the incoming sync signals (PLL) and passing the resulting digital data to the digital part of the

board. The digital part of the board is responsible for determining which pixel to capture and which ones to ignore, generating sync and other I/O signals, buffering incoming data and handling the DMA of image data into the host.

The following subsections describe each component in more detail.

1.4.1 Video Connector

The Video Connector is a 62-pin, 3-row female D-sub type connector. All of the video signals are located on this connector as well as all of the I/O signals. Unlike other BitFlow frame grabbers, there is not a separate I/O connector. This connector also supplies 12V DC to power small cameras. Keep in mind the same connector is used for all four VFGs (in the case of the ALT-PCE-AN4). Even though each VFG has the same block diagram, each one is connected to different pins on the Video Connector. See Section 10.2 for pin-out information.

1.4.2 Video Router

The Video Router is responsible for passing the correct video input pin to the correct A to D converter. Each VFG has four video inputs, but only three A-to-D converters. Depending on the type camera, single tap, dual tap, color, the routing has to be set appropriately. Also, the video router has a MUX function, which will let the board switch between two one tap or two tap cameras.

1.4.3 The A-to-D Converters

The A-to-D converters are 8-bit, low noise, high speed analog to digital converters. This converters turn the analog signal from your camera into a digital signal which can then be transferred to memory in your computer. For more details about the converters see Section 9.1.

1.4.4 Data Mux, Data Converter, FIFO

This block is very similar to all of the modern BitFlow frame grabbers (i.e. The R64, Karbon and Neon). This block aligns and packs the incoming data. The data can be shifted, masked, windowed and many other operations in this block.

1.4.5 Digital PLL

The Digital PLL (Phase Lock Loop) is used to recover the pixel clock from the camera's sync information. The sync information is either embedded in the video signal, or comes into the board as separate sync signals. In order to digitize the analog video, a pixel clock is required. Since the analog video standards to not provide a clock, the clock must be reconstructed on the frame grabber. The digital PLL is capable of creating clocks for a wide variety of different resolutions and frequencies. The parameters

in the camera configuration file tell the PLL what frequency clock is needed. Of course, this frequency must match exactly that of the camera in order to get correct aspect ratio images.

1.4.6 Signal Generator

The signal generator is used for a variety of purposes. It can generate signals that can control the camera. For example, when the camera is in async reset mode, the signal generator can generate a signal which tells the camera to reset and dump out another frame. This signal can be free running or tied to a trigger. The signal generator can also generate other signals to control external devices like strobes or actuators. The signal generator is fully programmable from software and/or from camera configuration files.

1.4.7 Scatter-Gather DMA Engine, PCIe interface

The Scatter-Gather DMA engine is one of the most powerful parts of the Alta. The DMA engine is responsible for moving image data from the frame grabber into the computers host memory. DMA engines can move one chunk of data without using the CPU. Scatter-gather DMA engines move unlimited amounts of data without using the CPU. This latter type is very important in imaging applications as the CPU is usually required for image processing.

The PCIe interface is used to setup and control the board. Host commands (from user applications) are send out on the PCIe bus. The board's PCIe interface receives the commands and passes them onto the appropriate part of the board. Each board get's assigned its own address space(s). When an application send, for example, a grab command to the board, the driver actually ends up interpreting this command as a memory write to the board's address space. The board see the write cycle, picks up the incoming data, and take appropriate action. In the case, the grab command will start the board acquiring image.

1.5 The Alta-AN Models

There are three models in the Alta-AN family, the ALT-PCE-AN1, ALT-PCE-AN2 and the ALT-PCE-AN4. Table 1-1 illustrates the capabilities of each model.

Table 1-1 Alta-AN Model Comparison

Parameters	ALT-PCE-AN1	ALT-PCE-AN2	ALT-PCE-AN4
Number of simultaneous monochrome cameras	1	2	4
Number of simultaneous two-tap cameras	1	2	4
Number of simultaneous RGB cameras	1	2	4
Number of A to Ds	3	6	12
Number of trigger inputs	1	2	4
Total number of camera muxed	2	4	8

Acquisition and Camera Control

Chapter 2

2.1 Introduction

This section covers acquisition and camera control for the R64-CL, Karbon-CL, Neon-CL and the Alta-AN.

2.2 BitFlow's Flow-Thru Architecture

The MUX component of the block diagrams for the Alta, Karbon, Neon and R64 is composed of a chain of sub-blocks that make up the Flow-Thru Architecture (FTA). Figure 2-1 shows the structure of the FTA for the Camera Link boards. Figure 2-2 shows the structure of the Alta family. All the data paths are 64-bit. The implementation of the individual blocks depends on the camera format, i.e. it is specific to the firmware downloaded for each sensor architecture. There is a bitfield, FORMAT, which indicates the currently downloaded firmware.

Below is a description of the individual blocks. For each block are shown the signals that are defined by the user.

Data from the Camera Link or AFE is synchronized and assigned to data lanes according to the camera format. The user has no control over these operations. From this block the data goes to a Barrel Shifter.

The Barrel Shifter is composed of four 16-bit barrel shifters. All shifters receive the same command, Left/Right and the amount of shift, up to 15 bits. The main purpose of the Barrel Shifter is for cameras that have more than 8 bits per pixel. The Barrel Shifter can down-shift the data to 8-bit suitable for display. Any camera with up to four taps can be accommodated.

There is a Video Delay Line (not shown) in the data path which can delay the video by up to 8 clocks. This is useful for accurate alignment of the video on the display.

The Video Selector selects the data source: the video from the camera or the on-board generated synthetic video. The various patterns of synthetic video are useful mainly for the on-board Built In Self Test (BIST).

The Mask is a 32-bit mask replicated over the upper and lower 32 bits of the 64-bit data path. The purpose of this mask is to be able to set to zero any bit in the data path (a one will pass the data as is, a zero will set that bit to zero).

The Clip is a clipping mechanism replicated on each one of the eight 8-bit data lanes. If enabled, it will clip the 256 gray levels in each lane according to the formula:

If video > 245 then video = 245
If video <10 then video = 10

This mechanism is useful for displaying gray level data on a VGA that is set in 256-color mode. In this mode the upper and lower 10 gray levels are dedicated to the Windows graphics.

The Assembler will assemble and pack the video data before it is written in the FIFO. This block does the raster scan re-arranging of the data. The packing is dependent on the pixel depth, which is defined in the PIX_DEPTH bitfield in CON10. The DISPLAY bit will force this block to assemble the data as 8-bit pixels, suitable for display. When using this mode, the barrel shifters must be set to down-shift each pixel by the correct amount. A 10-bit camera, for example, would need a 2-bit right shift.

The SWAP bit will swap between odd-even data streams for cameras that supply odd-even pixels.

The amount of data written in the FIFOs is controlled by the Acquisition Window. The vertical and horizontal size of this window is programmed in the ALPF and the ACLP registers respectively (see Section 2.4). The timing of this window is determined by the camera and the acquisition state machine.

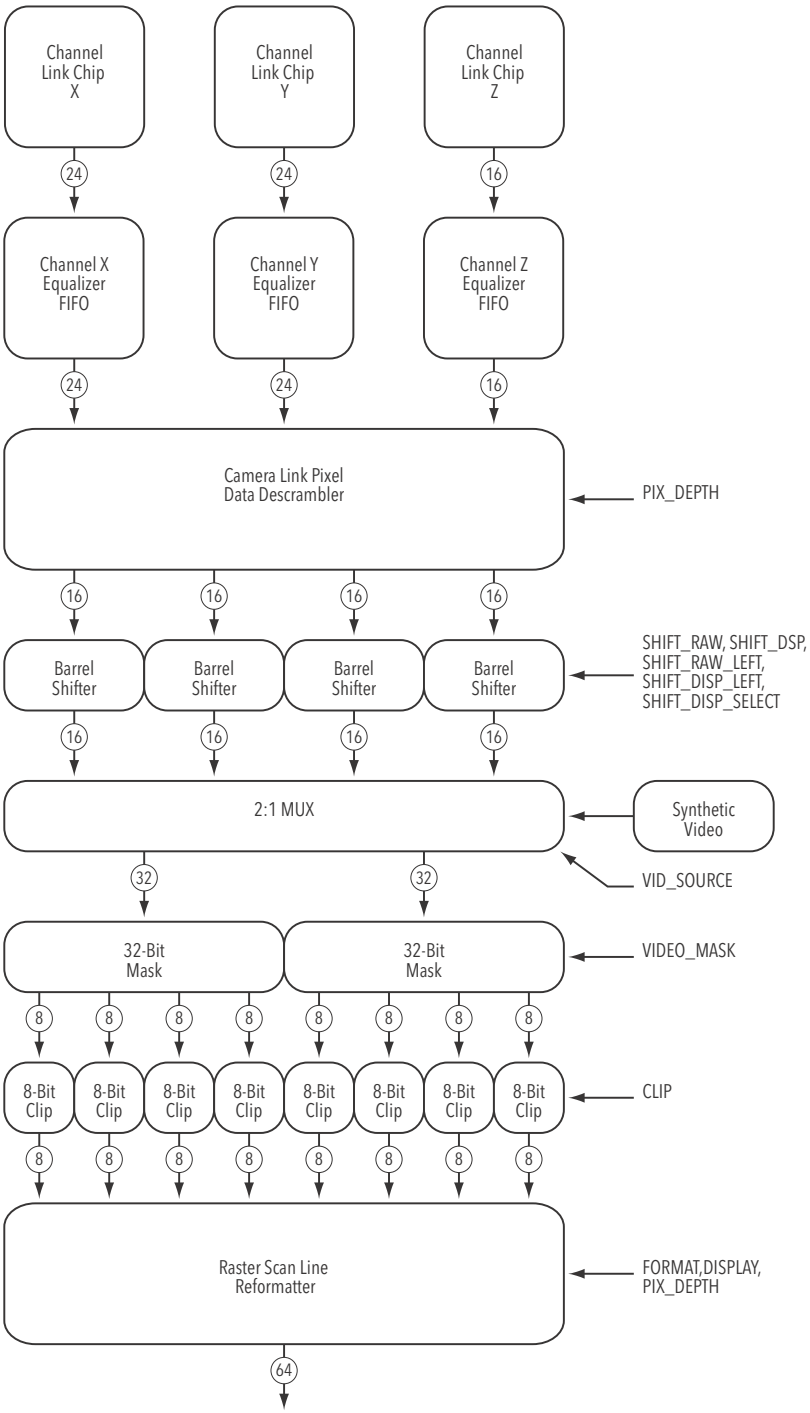

Figure 2-1 Flow Thru Architecture - R64, Karbon and Neon

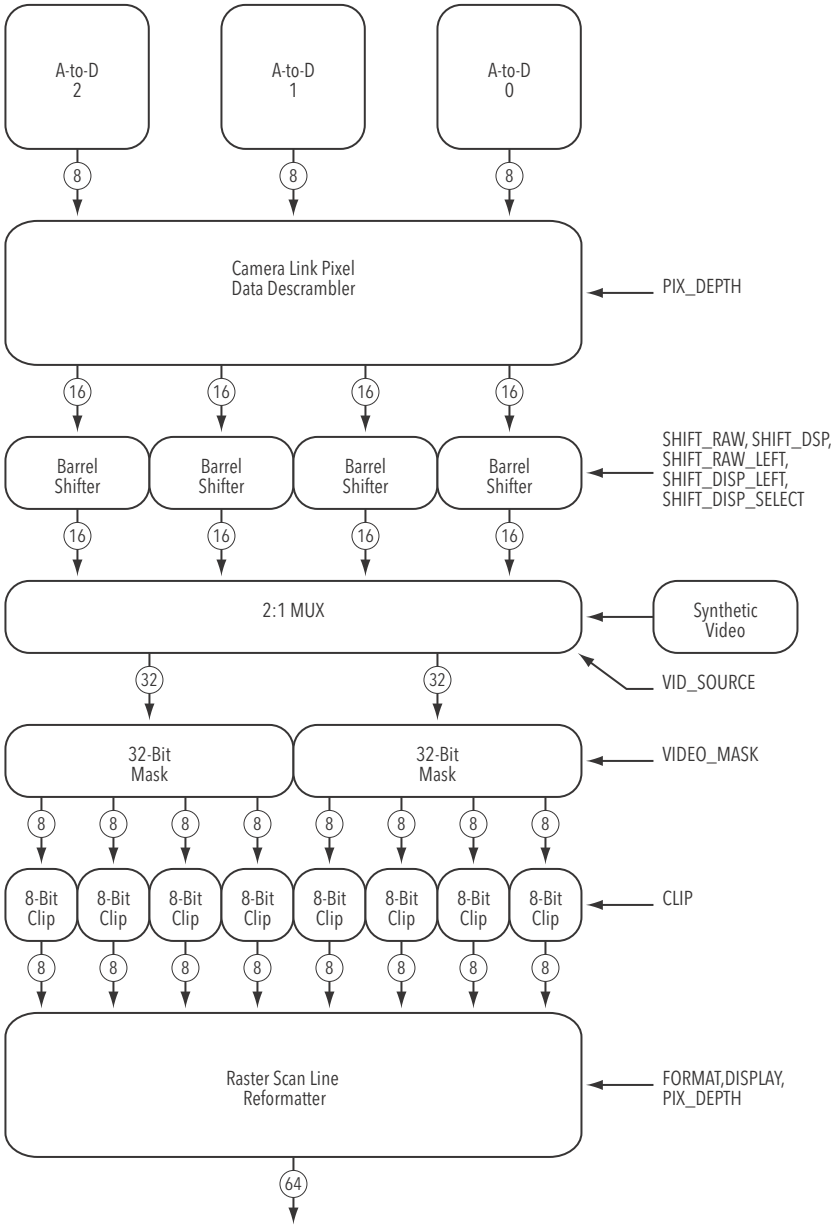

Figure 2-2 Flow Thru Architecture - Alta

2.3 Camera Specific Firmware

The Flow-Thru architecture is flexible and can be adapted to different cameras architectures. The main intelligence is in the firmware that gets downloaded into the on-board Field Programmable Gate Arrays (FPGAs). This firmware is different for every camera architecture. The firmware is called out in the camera file. On initialization, the driver will download into the FPGAs the firmware called-out in the camera file.

The type of the firmware is hard-coded in the FORMAT field in register CON10. The list of the formats is shown in Table 2-1

Note: Not all models support all formats. Only formats that are possible are supported. For example, the Neon, which is Base Camera Link only, will not support the MUX_8TS format as the is a Full Camera Link format.

Table 2-1 Firmware Options

FORMAT	Firmware Name	Format Description
0	MUX	1 tap cameras
1	MUX_2TOEP	2 taps, odd-even pixels
2	MUX_2TOEL	2 taps, odd-even lines
3	MUX_2TS	2 taps, segmented
4	MUX_2TS1RI	2 taps, segmented, right inverted
5	MUX_4TS	4 taps, segmented
6	MUX_4T2S2RIOEP	4 taps, odd-even pixels, right taps inverted
7	MUX_4TQ2RI2BU	4 quads, right quads inverted, bottom quads upside down
8	MUX_2CAM	2 cameras: 1 tap each
9	MUX_2CAM_2TOEP	2 cameras: 2 taps, odd-even pixels
10	MUX_2CAM_2TS1RI	2 cameras: 2 taps, segmented, right-inverted
11	MUX_2CAM_2TS	2 cameras: 2 taps, segmented
12	MUX_2CAM_2TOEL	2 cameras: 2 taps, odd-even lines
13	MUX_8TS	8 taps, segmented
14	MUX_BAY	Bayer decoder, 1 tap 8 bit
15	MUX_BAY_OE	Bayer decoder, 2 taps, odd-even pixels
16	MUX_BAY_2TS	Bayer decoder, 2 taps, segmented
17	MUX_4WI	4 taps, 4-way interleaved
18	MUX_2TOEPI	2 taps, odd-even pixels, both inverted
19	MUX_1TI	1 tap, inverted

Table 2-1 Firmware Options

FORMAT	Firmware Name	Format Description
20	MUX_8WI	8 taps, 8-way interleaved
21	MUX_BAY_2TS_RI	Bayer decoder, 2 taps, segmented, right inverted
22	MUX_4TS2RI	Four taps, segmented, right two taps inverted
23	MUX_8TSOEP4RI	Eight taps, segments, odd/even pixel, for right taps inverted
24	MUX_10WI	Ten taps, interleaved

2.4 Generation of Acquisition Windows

2.4.1 The Horizontal Active Window, HAW

The Horizontal Active Window (HAW) is a square wave that defines the portion of the line that will be acquired horizontally. HAW can span less than the whole camera line, if we want to acquire only a portion of that line. The size of the HAW is determined by a single number, the Active Clocks Per Line (ACPL). The ACPL is defined as the number of clocks during which the HAW is active. The ACPL field is programmed in CON10. The 17 bits define the maximum HAW as minimum 128K pixels.

The total number of pixels per line that will be acquired can be different than the ACPL. For a dual tap camera that supplies odd-even pixels for example, the total number of pixels acquired will be twice the ACPL, as for every clock the camera supplies two pixels. Note that the ACPL is not a function of the bits per pixel. The relationship between the number of pixels per line and the number of clocks per line is controlled by the firmware currently downloaded to the board. The FORMAT register will indicate which firmware is currently downloaded. Each tap configuration requires a different firmware file be downloaded. The correct firmware is automatically downloaded based on the information contained in the camera configuration file.

The size of the HAW is on an arbitrary boundary. The start in time of the HAW can come from two sources, depending on the setting of the HAW_START bit:

The HSTART bit in the HCTAB, if HAW_START = 1.
The start of LEN, if HAW_START = 0.

In both modes, the start of the HAW can be delayed 0-7 clocks relative to the start function (HSTART or LEN). This is done by the TRIM bits in CON9.

In both modes, the start of the HAW can be advanced 0-7 clocks relative to the start function (HSTART or LEN). This is done by the DELAY bits in CON14.

The HCTAB is the Horizontal Control Table that generates the HSTART, see section on CTABs.

Figure 2-3 shows the controls that generate the HAW.

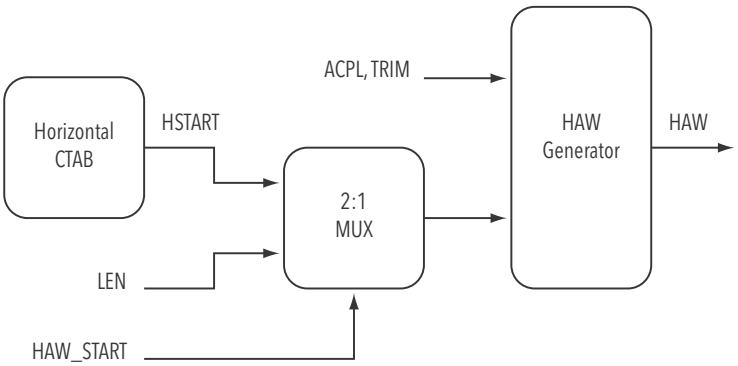

Figure 2-3 Generation of the Horizontal Active Window, HAW

2.4.2 The Vertical Active Window, VAW

The Vertical Active Window (VAW) is a square wave that defines the portion of the frame that will be acquired vertically. VAW can span less than the whole camera frame, if we want to acquire only a portion of that frame. The size of the VAW is determined by a single number, the Active Lines Per Frame (ALPF). The ALPF is defined as the number of HAW periods during which the VAW is active. The ALPF field is programmed in CON17. The 17 bits define the maximum VAW as minimum 128K lines.

The total number of lines per frame that will be acquired can be different than the ALPF. For a dual tap camera that supplies odd-even lines for example, the total number of lines acquired will be twice the ALPF as in the period of one HAW the camera supplies two lines.

The size of the VAW is on an arbitrary boundary. The start in time of the VAW can come from two sources, depending on the setting of the VAW_START bit:

The VSTART bit in the VCTAB, if VAW_START = 1.
The start of FEN, if VAW_START = 0.

Data will be acquired in the window defined by the HAW and the VAW

Figure 2-4 shows the controls that generate the VAW.

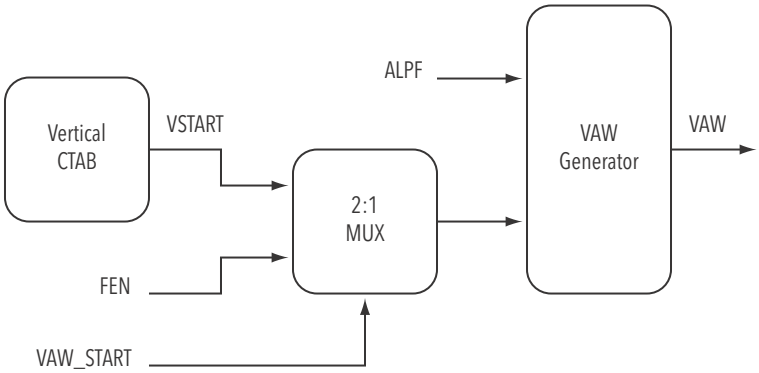

Figure 2-4 Generation of the Vertical Active Window, VAW

2.5 The Control Tables (CTABs)

The CTABs are two memories that are programmed by the host computer and read by the board's acquisition circuitry. The read-out is done in a sequential fashion, i.e. the memories' addresses are scanned sequentially. There is a vertical' memory (VCTAB) and a horizontal' memory (HCTAB). The vertical and horizontal memory each has an associated counter which scans its addresses, VCOUNT and HCOUNT respectively. The concept here is similar to how a CPU runs a program. There is a PC which works it's way through memory, processing each instruction in turn. Each bit in the CTAB corresponds to a different operation. For example, one bit might control the level of a signal going to the camera. In this case the CTABs can be thought of as programmable waveform generators. Another bit might cause an interrupt to occur on the PCI bus, yet another bit might force the HCOUNT to go to zero. The CTABs are fully programmable by software. The details of the CTABs are describe in this section.

2.5.1 Vertical Control Table

Figure 2-5 depicts the structure of the Vertical Control Table (VCTAB). For clarity, the address and data path that allow the host to program the VCTAB are not shown.

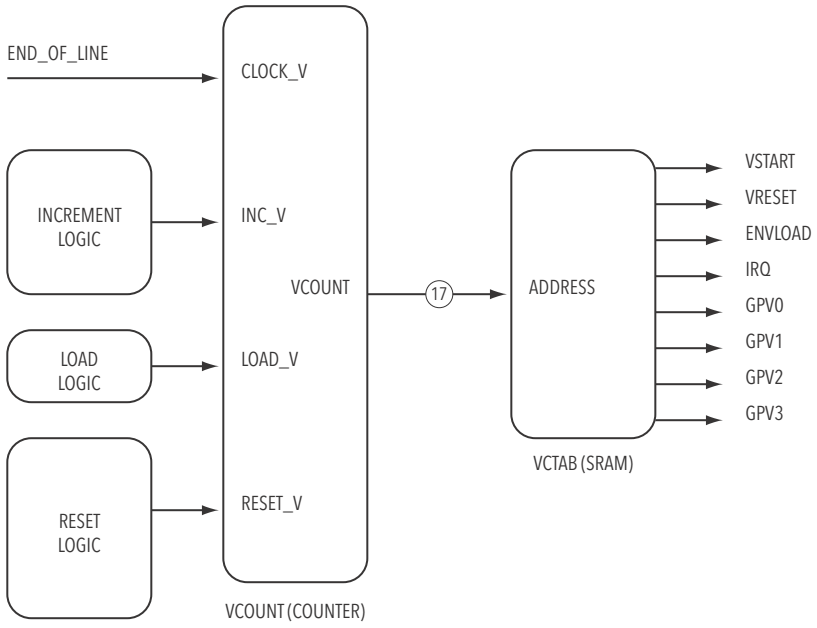

Figure 2-5 Vertical Control Table

The Vertical Control Table is made up of the following blocks:

VCOUNT - a synchronous counter that can be incremented, loaded and reset. The clock that drives VCOUNT is derived from the HCTAB, see below. VCOUNT is 17-bit wide and is connected to the address input of the VCTAB.

Logic for generating INC_V - the increment control signal to the VCOUNT.

Logic for generating LOAD_V - the load control signal to the VCOUNT. When LOAD_V is asserted, VCOUNT is loaded with the value of 8000h (32,768 in decimal).

Logic for generating RESET_V - the reset control signal to the VCOUNT. When RESET_V is asserted, VCOUNT is reset to 0.

Logic for generating CLOCK_V - the clock to the VCOUNT.

VCTAB - a static memory (SRAM) that outputs eight VCTAB control signals. The address of this SRAM is driven by VCOUNT.

If RESET_V and LOAD_V are asserted simultaneous, RESET_V overrides.

As the VCOUNT increments, it scans the addresses of the VCTAB in ascending order. The output of the VCTAB depends on the data that has been written in the VCTAB by the host. If the VCOUNT is free running, it will cyclically scan all the VCTAB's addresses. Any arbitrary cyclic waveform can be implemented by programming the VCTAB with the adequate data.

The LOAD_V and RESET_V will enable the synchronization between external events and the waveforms generated by the VCTAB. LOAD_V and RESET_V will force the VCOUNT to known values, 8000h and 0 respectively.

The INC_V signal will allow for stopping the counter from incrementing. In that case, the output of the VCTAB will be constant. While the VCOUNT is not incrementing, it can still be loaded or reset, see the logic below.

2.5.2 The VCTAB Functions

The functions assigned to the columns in the VCTAB are shown in Table 2-2.

Table 2-2 The VCTAB Functions

Bit	Name	Function
0	VSTART	Start of VAW
1	VRESET	Vertical Reset
2	ENVLOAD	FEN Mask, enable load
3	IRQ	CTAB Interrupt
4	GPV0	General purpose vertical function 0
5	GPV1	General purpose vertical function 1
6	GPV2	General purpose vertical function 2
7	GPV3	General purpose vertical function 3

VSTART defines the start of the Vertical Acquisition Window (VAW), if the start is provided by the VCTAB, see previous section.

VRESET defines the reset of the VCOUNT, in case this function is programmed in the VCTAB.

ENVLOAD enables the FEN to load the VCOUNT. The rationale behind the ENVLOAD column from the VCTAB is that some cameras might not give a FEN, but only two pulses: the start and end of FEN. With the ENVLOAD, we can mask out the unwanted one.

IRQ provides an interrupt to the host, allowing an interrupt to occur at any point on the vertical axis.

GPV are general purpose vertical functions, see usage below.

Note: If a VRESET pulse happens coincident with a LOAD, the LOAD is overriding.

The CLOCK_V Control

CLOCK_V is the clocking of the VCOUNT is generated by the end of the line (horizontal reset).

The INC_V Control

INC_V is the logic for incrementing VCOUNT.

There are only two instances when we want to inhibit the incrementing of VCTAB. The first instance is when VCOUNT reaches 0000h, the "Stop at Zero" case. The other instance is when VCOUNT reaches 7FF0h, the "Vertical Stick" case.

Stop at Zero

Usually, VCOUNT will reach zero because of a RESET_V signal. After VCOUNT is reset, there are programmable options defined by VCNT_RLS_ZERO. Depending on this bitfield, VCOUNT can continue to count or wait at zero till some event occurs, usually the assertion of the TRIGGER.

This operating mode is especially useful for synchronizing cameras to external events. TRIGGER is usually the output of a part-in-place signal. Until this signal is asserted, the VCOUNT waits at address 0000h. After the TRIGGER is asserted, VCOUNT starts counting, i.e., scanning the VCTAB in ascending order. At some address we will program a sync signal to be sent to the camera, usually through GPV0. In response to this sync signal, the camera will give back a frame, and it will assert FEN. The FEN will load address 8000h into VCOUNT. In the VCTAB, we will program the vertical acquisition window to start after address 8000h. At the end of the vertical acquisition window the RESET_V will be asserted, which in turn will reset the VCOUNT. VCOUNT will wait at address 0000h until TRIGGER is asserted.

Vertical Stick

Using the previous example, assume that after we asserted the sync signal to the camera, we expect the camera to give us a frame, i.e., assert FEN. While we expect the camera to assert FEN, VCOUNT is still being incremented. If it takes too long for the camera to respond, VCOUNT will eventually reach and pass beyond 8000h. A vertical

acquisition window will be asserted, even though the camera did not assert FEN. To avoid such a situation, just before address 8000h, when VCOUNT reaches 7FF0h, it will stop. It will stay at 7FF0h until FEN is asserted. Then, VCOUNT will be loaded with 8000h.

The Vertical Stick will occur according to the setting of VCNT_RLS_STK.

The LOAD_V Control

LOAD_V is the logic of loading VCOUNT. In other words, loading VCOUNT means it jump to a new address.

VCOUNT will be loaded with the value 8000h by the rising/falling edge of FEN, if ENVLOAD is asserted. FEN usually marks the start of a valid frame. The start of the vertical acquisition window can be placed starting at address 8000h.

ENVLOAD is a column in the VCTAB. There are cameras that do not assert FEN. Some other type of cameras assert only the start and stop of a frame. In this case, ENVLOAD can mask out the unwanted signals.

Operation on the rising/falling edge of FEN is selected by FENPOL, see CON14

The RESET_V Control

RESET_V is the logic of resetting VCOUNT.

VCOUNT can be reset from different sources, under different conditions. The resetting of the VCOUNT is controlled by the VCNT_RST bitfield.

2.5.3 Vertical Control Table Size

The Vertical Control Table has 20000h (131,972) entries.

2.5.4 Horizontal Control Table

The Horizontal Control Table (HCTAB) is 8 bits wide. The function of each bit is show in the following table.

Figure 2-6 depicts the structure of the HCTAB. For clarity, the address and data path that allow the host to program the HCTAB are not shown

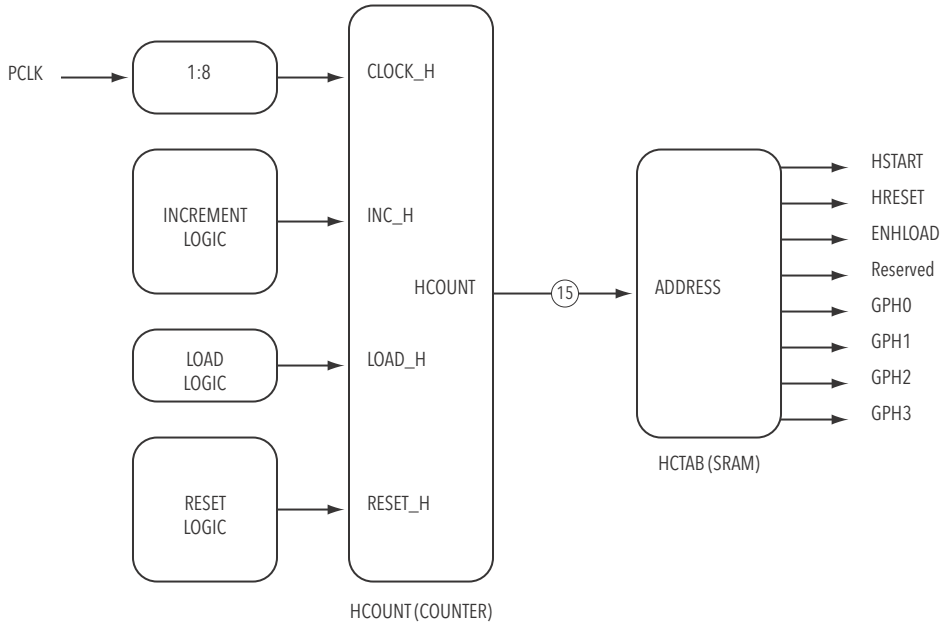

Figure 2-6 Horizontal Control

The Horizontal Control Table is made up of the following blocks:

HCOUNT - a synchronous counter that can be incremented, loaded and reset. The clock that drives HCOUNT is a free running clock, PCLK/8, i.e., the pixel clock divided by eight. HCOUNT is 15 bits wide and is connected to the address input of the HCTAB.

The 15 bit HCOUNT with the PCLK/8 can generate functions up to 256K PCLKs long, on boundaries of 8 PCLKs.

The ACPL is 17 bit, and that can generate an HAW of up to 128K PCLKs.

Logic for generating INC_H - the increment control signal to the HCOUNT.

Logic for generating LOAD_H - the load control signal to the HCOUNT. When LOAD_H is asserted, HCOUNT is loaded with the value of 2000h.

Logic for generating RESET_H - the reset control signal to the HCOUNT. When RESET_H is asserted, HCOUNT is reset to 0.

HCTAB - a static memory (SRAM) that outputs eight HCTAB control signals. The address of this SRAM is driven by HCOUNT.

Logic for generating CLOCK_H - the clock to the HCOUNT. This is a frequency divider. CLOCK_H is PCLK, the pixel clock divided by eight.

Note: If RESET_H and LOAD_H are asserted simultaneously, RESET_H overrides.

As the HCOUNT increments, it scans the address of the HCTAB in ascending order. The output of the HCTAB depends on the data that has been written in the HCTAB by the host. If the HCOUNT is free running, it will cyclically scan all the HCTAB's addresses. Any arbitrary cyclic waveform can be implemented by programming the HCTAB with the adequate data.

The LOAD_H and RESET_H will enable the synchronization between external events and the waveforms generated by the HCTAB. LOAD_H and RESET_H will force the HCOUNT to fixed values, 2000h and 0 respectively.

The INC_H signal will allow for stopping the counter from incrementing. In that case, the output of the HCTAB will be constant. While the HCOUNT is not incrementing, it can still be loaded or reset, see the logic below.

2.5.5 The HCTAB Functions

The functions assigned to the columns in the HCTAB are shown in Table 2-3.

Table 2-3 The HCTAB Functions

HCTAB	Name	Function
D0	HSTART	Start of HAW
D1	HRESET	Reset HCOUNT and increment the VCOUNT
D2	ENHLOAD	LEN Mask, enable horizontal load
D3	reserved	
D4	GPH0	General purpose horizontal function 0
D5	GPH1	General purpose horizontal function 1
D6	GPH2	General purpose horizontal function 2
D7	GPH3	General purpose horizontal function 3

HSTART marks the start of the Horizontal Acquisition Window, HAW. Video will be acquired only while the HAW is active.

HRESET will reset the HCOUNT.

ENHLOAD will allow the loading of the HCOUNT. A location that has 1 will allow the loading of the HCOUNT. A 0 will inhibit the loading of the HCOUNT.

GPH are general purpose horizontal functions. See usage below.

The INC_H Control

INC_H is the logic for incrementing HCOUNT.

There are only two instances when we want to inhibit the incrementing of HCTAB. The first instance is when HCOUNT reaches 0000h, “Stop at Zero” case. The other instance is when HCOUNT reaches 1FF1h, the “Horizontal Stick” case.

The "Stop at Zero" Case

Usually, HCOUNT will reach zero because of a RESET_H signal. After HCOUNT is reset, there are two programmable options:

HCOUNT keeps on counting.
HCOUNT stays at zero until ENCODER is asserted.

The selection between the two options is done by the HCNT_RLS_ZERO bitfield, see next section on camera synchronization.

This operating mode is especially useful for synchronizing line scan cameras to external events. ENCODER is usually the output of an encoder or a tachometer signal. Until this signal is asserted, the HCOUNT waits at address 0000h. After the ENCODER is asserted, HCOUNT starts counting, i.e., scanning the HCTAB in ascending order. At some address we will program a sync signal to be sent to the scan camera, usually through GPH0. In response to this sync signal, the camera will give back a line, and it will assert LEN. The LEN will load address 2000h into HCOUNT. In the HCTAB, we will program the horizontal acquisition window after address 2000h. At the end of the horizontal acquisition window the RESET_H will be asserted, which in turn will reset the HCOUNT. HCOUNT will wait at address 0000h until ENCODER is asserted.

Horizontal Stick

Using the previous example, assume that after we asserted the sync signal to the camera, we expect the camera to give us a line, i.e., assert LEN. While we expect the camera to assert LEN, HCOUNT is still being incremented. If it takes too long for the camera to respond, HCOUNT will eventually reach and pass beyond 2000h. A horizontal acquisition window will be asserted even though the camera did not assert LEN. To avoid such a situation, just before address 2000h, when HCOUNT reaches 1FF0h, it will stop. It will stay at 1FF0h until LEN is asserted. Then, HCOUNT will be loaded with 2000h.

The LOAD_H Control

LOAD_H is the logic of loading HCOUNT.

HCOUNT will be loaded with the value 2000h by the rising/falling edge of LEN, if ENHLOAD is asserted. LEN usually marks the start of valid data in a line. The Horizontal Acquisition Window can be placed starting at address 2000h.

ENHLOAD is a column in the HCTAB that enables the LEN. There are cameras that do not assert LEN. In that case, the LEN input must be disabled, otherwise its behavior is unpredictable.

Operation on the rising/falling edge of LEN is selected by LENPOL, see CON14.

The RESET_H Control

RESET_H is the logic of reset HCOUNT.

HCOUNT can be reset from several sources, according to HCNT_RST bitfield, see next section on camera synchronization.

Example

Lets look at a simple example to clarify the concept of the HCTAB. Assume we want to program a free running horizontal window of 32 pixels active area. Just before the active area we want to fire a strobe using GPH0. D0 (HSTART) defines the start of the HAW. Bit D1 defines the reset of the HCOUNT. D4, GPH0, is the strobe pulse. The size of the HAW is programmed in ACLP register.

Taking into account that the address counter is clocked by 1/8 the pixel clock, the HCTAB memory map will be as shown in Table 2-4.

Table 2-4 HCTAB Example

HCTAB Address	HRESET	HSTART	GPH0	Comments
0	0	0	0	You got here from address 9
1	0	0	0	
2	0	0	0	
3	0	0	1	Fire the strobe
4	0	1	0	Start Horizontal Acquisition Window
5	0	0	0	Acquire
6	0	0	0	Acquire
7	0	0	0	Acquire
8	0	0	0	Acquire
9	1	0	0	Assert RESET_H
10	0	0	0	

The CT Functions

The CT's are four functions derived from the HCTAB and the VCTAB. Those functions can define an arbitrary horizontal and/or vertical waveform. The definition of the CT's is given below:

CT[0] = GPV[0] AND GPH[0]
CT[1] = GPV[1] AND GPH[1]
CT[2] = GPV[2] AND GPH[2]
CT[3] = GPV[3] AND GPH[3]

Each CT has a vertical and a horizontal component. Both components are programmed in the CTABs. The minimum horizontal pulse is 8 PCLKs. The minimum vertical pulse is one line.

The CT's can be steered to the Camera Controls (on the CL connectors) and to the GPOUTs, on the IO connector.

2.5.6 Horizontal Control Table Size

The Horizontal Control Table has 8000h (32,768) entries.

2.6 Synchronizing Acquisition, Camera, CTABs and External Signals

These boards have extremely flexible camera interfaces. They have been designed to acquire from almost any Camera Link camera and to synchronize with almost all industrial signals. There are two layers of synchronization. The first layer is to synchronize to signals coming from the industrial environment. For example triggers and encoders. The second layer is to synchronize to the camera. This requires both sending signals to the camera (e.g. exposure control) and receiving signals from the camera (e.g. Pixel Clock, Line Enable and Frame Enable). All of these synchronization problems are solved by the Control Tables (CTABs) and Vertical/Horizontal Operations. See previous section for detailed operation on the CTABs.

The Vertical and Horizontal Operations describe different state changes that the board goes through. For example one operation might be to begin acquiring pixels, another might be to reset the VCOUNT back to zero. Generally these state changes are caused by one or more events. There are a number of events, both horizontal and vertical, that the board can react to. These events are tied to operations by a set of programmable bitfields. The details of these events are outlined in this section.

2.6.1 Vertical Operations and Events

The vertical operations are related to the vertical axis of an image (in memory or on the display) or frame timing (of a camera). The operations are mainly commands to VCOUNT and acquisition commands. Each operation can be initiated by some event. The selection of the event that will initiate the specific operation is done by a set of three control bits related to each operation.

Table 2-5 is a list of the vertical operations and their related control bits.

Table 2-5 Vertical Operations

Vertical operation	Control bits
VCOUNT frozen/released from 0000h	VCNT_RLS_ZERO
VCOUNT reset to 0000h	VCNT_RST
VCOUNT load with 8000h	VCNT_LD
VCOUNT frozen/released from 7FF0h	VCNT_RLS_STK
VCOUNT increment	VCNT_INC
Acquire (SNAP, GRAB, CONTINUOUS)	ACQ_CON
FREEZE acquisition	FREEZE_CON
ABORT acquisition	ABORT_CON
START vertical acquisition window	VAW_START

Table 2-6 is a list of the events that initiate the vertical operations:

Table 2-6 Vertical Events

Event description	Event Name
TRIGGER asserted	TRIG_ASRT
TRIGGER de-asserted	TRIG_DASRT
FEN asserted	FEN_ASRT
FEN de-asserted	FEN_DASRT
TRIGGER is HI	TRIG_HI
TRIGGER is LO	TRIG_LO
RESET from VCTAB	RST_VCTAB
RESET from SW	RST_SW
Host writes acquisition command	HOST_WCMD_GRAB/SNAP
Acquisition frame counter reaches programmed value	AQ_COUNT

What follows is a list of each operation and the corresponding events that can be used to cause the operation. Included is the bitfield settings for each operations. It is important to understand that each operation is independent and can be programmed without regard for how the other events are programmed. However, some combinations might not make sense.

VCOUNT Release From Zero

This operation controls the behavior of VCOUNT when it reached zero. See Table 2-7.

Table 2-7 VCNT_RLS_ZERO

Initiator	VCNT_RLS_ZERO	Comments
None	0	Normal operation mode, no stop at 0000h
TRIG_ASRT	1	Edge Mode (aka Letter Mode), always stay at 0000h, release on TRIG_ASRT
TRIG_HI	2	Level Mode (aka Luggage Mode), stay at 0000h if TRIG_LO, release on TRIG_ASRT

VCOUNT Reset To Zero

This operation controls how VCOUNT is reset to zero. See Table 2-8.

Table 2-8 VCNT_RST

Initiator	VCNT_RST	Comments
End_of_VAW	0	Default operation, reset at end of VAW
TRIG_DASRT or End_ of_VAW	1	Triggered termination
RST_VCTAB	2	Reset from VCTAB
FEN asserted or	3	Reset from start of FEN
TRIG_DASRT or RST_ VCTAB	4	Triggered termination
TRIG_DASRT	5	Triggered termination

Note: The VCOUNT is always reset by the RST_SW (sofware reset) and by the HOST_ WCMD_ABORT (host writes ABORT command).

VCOUNT Release From Stick Point (7FF0h)

This operation controls the behavior of VCOUNT when it hits the stick point. The purpose of the stick point is to allow for very long periods of time between frames. The stick point is located at 7ff0h. See Table 2-9.

Table 2-9 VCNT_RLS_STK

Initiator	VCNT_RLS_STK	Comments
None	0	Normal operation mode, no stop at 7FF0h
VLOAD or VRESET	1	Stick at 7FF0h till load (usually FEN) or reset asserted

VCOUNT Load To 8000h

This operation controls how and when VCOUNT loads (jumps to) 8000h. See Table 2-10.

Table 2-10 VCNT_LD

Initiator	VCNT_LD	Comments
None	0	No load
FEN_ASRT and ENV-LOAD	1	Assertion of FEN qualified with ENV-LOAD
FEN_ASRT	2	Assertion of FEN only
TRIG_ASRT	3	Assertion of TRIGGER

Acquisition Command Control

This operations controls how the acquisition commands get initiated. There are two major acquisition commands. The SNAP command, which only acquires one frame. The GRAB command, which continuously acquires frames until a freeze or abort command is issued. In addition, the board has a continuous data mode which is not frame oriented. In continuous data mode, the board will acquire data based only on the clock and data qualifying signals. There are no acquisition commands in this mode. See Table 2-11.

Table 2-11 ACQ_CON

Initiator	ACQ_CON	Comments
HOST_WCMD_GRAB/ SNAP	0	normal, host initiated GRAB/SNAP/ FREEZE
TRIG_ASRT	1	Triggered initiated GRAB/SNAP/ FREEZE
TRIG_ASRT and HOST_ WCMD_GRAB	2	Triggered SNAP
TRIG_HI	3	Continuous data, wo. CTABs

Note: See also Section 2.7 for more details on the how the acquisition commands work.

Freeze Command Control

This operation is used to stop acquisition when the board is in GRAB mode. Acquisition will stop immediately if the board is between frames, or at the end of the current frame, if the board is in the middle of a frame. See Table 2-12.

Table 2-12 FREEZE_CON

Initiator	FREEZE_CON	Comments
HOST_WCMD_ FREEZE	0	Normal, host initiated
AQ_COUNT or HOST_WCMD_ FREEZE	1	Acquisition counter reaches number of frames programmed in the AQ_COUNT register
TRIG_DASRT	2	Trigger de-asserted

Abort Command Control

This operations terminates the current acquisition immediately. This operation will terminate both a SNAP and a GRAB command. If the board is in the middle of a frame, only part of the frame will be acquired. See Table 2-13.

Table 2-13 ABORT_CON

Initiator	ABORT_CON	Comments
HOST_WCMD_ ABORT	0	Normal, host initiated
TRIG_DASRT or HOST_WCMD_ ABORT	1	Abort on falling edge TRIG or host command.

2.6.2 Horizontal Operations and Events

The horizontal operations and events are related to the horizontal axis (of an image in memory or on the display) or line timing (of a camera). The operations are mainly commands to HCOUNT. Each operation can be initiated by some event. The selection of the event that will initiate the specific operation is done by a set of three control bits related to each operation.

Table 2-14 lists the horizontal events.

Table 2-14 Horizontal Operations

Horizontal operation	Control bits
HCOUNT released from zero	HCNT_RLS_ZERO
HCOUNT reset to zero	HCNT_RST
HCOUNT load with 2000h	HCNT_LD
HCOUNT release from 1FF0h	HCNT_RLS7F0
HCOUNT increment	HCNT_INC
Start horizontal active window	HAW_START

The events that can initiate the horizontal operations are listed in Table 2-15.

Table 2-15 Horizontal Events

Event description	Event Name
ENCODER asserted	ENC_ASRT
ENCODER de-asserted	ENC_DASRT
LEN asserted	LEN_ASRT
LEN de-asserted	LEN_DASRT
ENCODER is HI	ENC_HI
ENCODER is LO	ENC_LO
RESET from HCTAB	RST_HCTAB
RESET from SW	RST_SW
FEN asserted	FEN_ASRT

The sections below enumerate all of the horizontal operations and how the various events can initiate them. The control of each operation is independent from all of the others.

HCOUNT Release From Zero

This operation controls the behavior of HCOUNT when it reached zero (see Table 2-16).

Table 2-16 HCNT_RLS_ZERO

Initiator	HCNT_RLS_ ZERO	Comments
None	0	Normal operation mode, no stop at zero
ENC_ASRT	1	One-shot mode, wait for encoder for release

HCOUNT Reset To Zero

This operation controls how HCOUNT is reset to zero (see Table 2-17).

Table 2-17 HCNT_RST

Initiator	HCNT_RST	Comments
END_OF_HAW	0	Default operation, end of HAW
FEN_ASRT or RST_ HCTAB	1	Reset on FEN_ASRT, Random FEN mode
RST_HCTAB	2	Reset from HCTAB

Note: The HCOUNT can always be reset by RST_SW or HOST_WCMD_ABORT

HCOUNT Release From Stick Point (1FF0h)

This operation controls the behavior of HCOUNT when it hits the stick point. The purpose of the stick point is to allow for very long periods of time between lines. The stick point is located at 1ff0h. See Table 2-18.

Table 2-18 HCNT_RLS_STK

Initiator	HCNT_RLS_STK	Comments
None	0	Normal operation mode, no stop at 1FF0h
HLOAD or HRESET	1	Stay at x1FF0 till load (usually LEN) or reset asserted

HCOUNT Load To 2000h

This operation controls how and when HCOUNT loads (jumps to) 2000h (see Table 2-19).

Table 2-19 HCNT_LD

Initiator	HCNT_LD	Comments
None	0	No load
LEN_ASRT	1	Load on LEN assert, qualified with ENH-LOAD column
ENC_ASRT	2	Load on ENCODER assert, qualified with ENHLOAD column

2.7 Acquisition Command and Status

This section describes how the acquisition state machine works. This state machine controls which frames from the camera are acquired and which are ignored. As the commands can be issued asynchronous to the camera's timing, the acquisition state machine will remember the command and execute it starting at the beginning of the frame. That will guarantee that whole frames will be acquired. Note that the acquisition state machine only marks the frames to be acquired. The amount of pixels/line and lines/frame to be acquired in the marked frame is determined by the HAW and VAW, see section Section 2.4.

The acquisition state machine is controlled by the following signals:

AQCMD, the acquisition command bitfield

VACTIVE, the camera's vertical active timing (usually FEN for area scan cameras)..

TRIGGER, the selected trigger.

ACQ_CON, a bitfield that defines special acquisition modes for the state machine.

The current state of the machine can be observed by the AQCMD and AQSTAT bitfields described below.

2.7.1 The Acquisition Bitfields

The acquisition command bits, AQCMD describe the command to be performed in the next frame. The acquisition status bits, AQSTAT, describe the current command that is performed. The four acquisition commands are described in the Table 2-20.

Table 2-20 ACQCMD

AQCMD	Command	Comment
0 (00b)	FREEZE	Stop acquiring at end of current frame
1 (01b)	ABORT	Stop acquiring immediately, unconditionally
2 (10b)	SNAP	Acquire one frame
3 (11b)	GRAB	Acquire continuously

The following list details the behaviors of these bitfields.

- The AQSTAT bits are set at the beginning of the VACTIVE. The last instance a command can be issued is about 4 LCLKs before the start of the VACTIVE.
- For a SNAP command, when the SNAP starts, the AQCMD bits are cleared. Note that for SNAP, the AQCMD bits are written by the host and cleared by the state machine.
- If during a SNAP/GRAB operation another SNAP/GRAB command is issued, it is ignored.

Table 2-11 below describes the acquisition modes for ACQ_CON

Table 2-21 ACQ_CON

ACQ_CON	Mode Description
0 (000b)	Host command performed on next frame
1 (001b)	Host command issued when TRIGGER asserted
2 (010b)	As long as GRAB command is on, a single frame will be SNAPped at every assertion of the TRIGGER.
3 (011b)	Continuous acquisition mode. Host commands are ignored. Data will be acquired continuously as long as the TRIGGER is asserted.

Figure 2-7 shows a timing diagram of the SNAP command, with ACQ_CON = 0. The command is written by the host during the active frame. The acquisition will start at the beginning of the next frame.

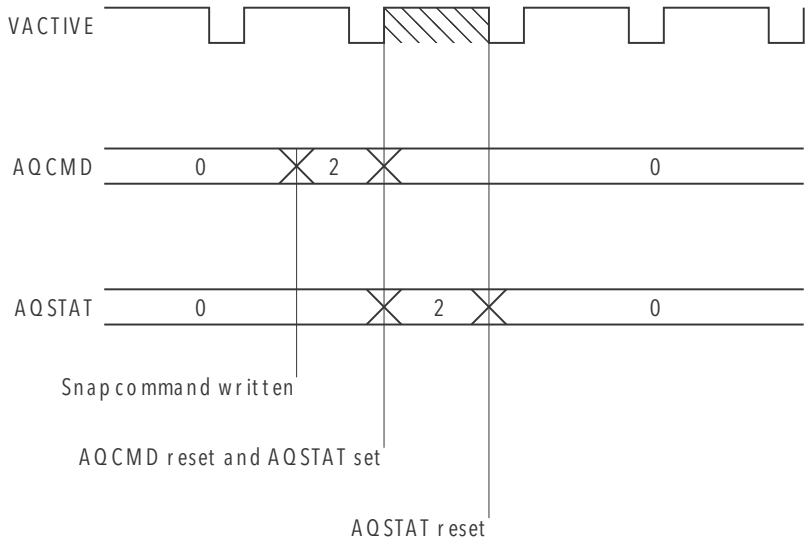

Figure 2-7 Snap Command Timing

Figure 2-8 shows the timing of the GRAB operation with ACQ_CON=0. Figure 2-9 shows the timing of the ABORT operation with ACQ_CON=0. Note that the ABORT command will cut off part of the frame. This command is useful for resetting the board without having to wait for the end of the frame. Figure 2-10 shows a SNAP operation with ACQ_CON=1. In this mode, after the TRIGGER has been asserted and the command executed, the host must write a new command in the AQCMD field. Figure 2-11 shows acquisition in ACQ_CON=2 mode. Here, as long as the GRAB command is on, a frame will be acquired for every assertion of the TRIGGER. In this mode, there is no need for the host to write a new command.

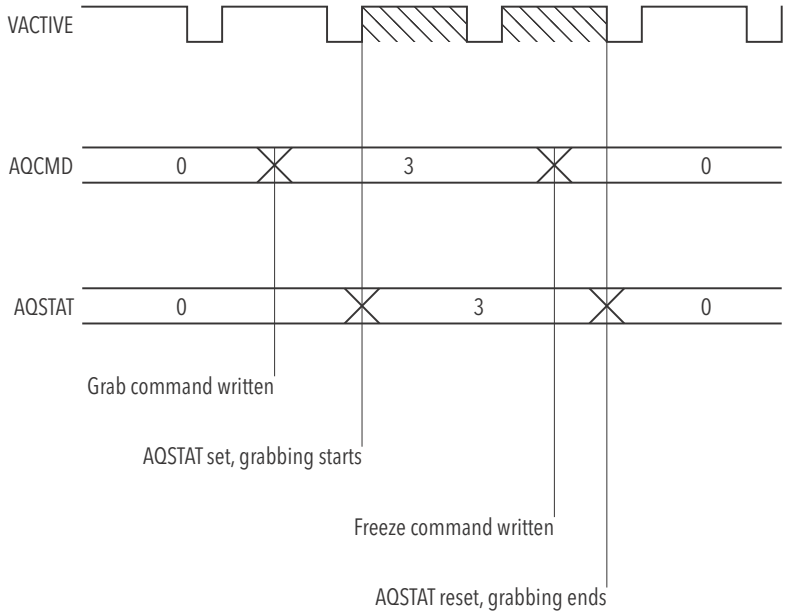

Figure 2-8 Grab Command Timing

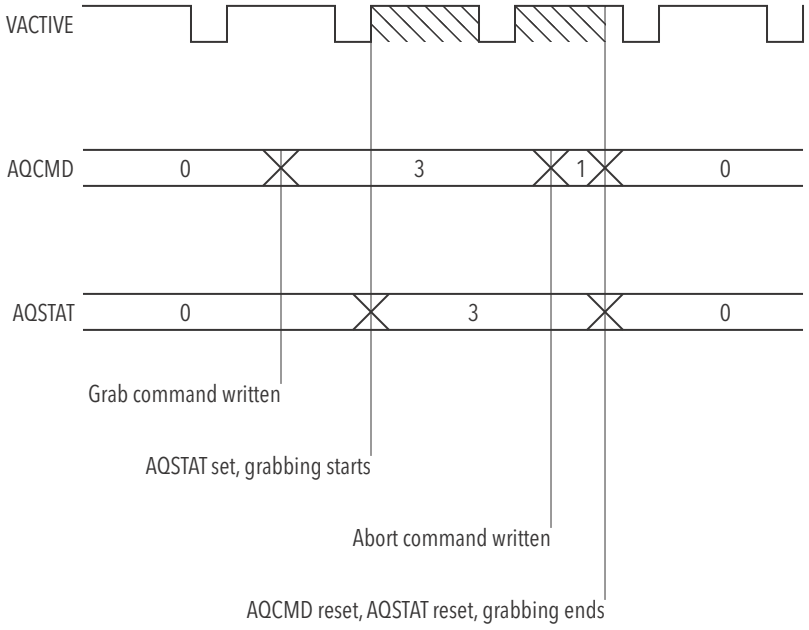

Figure 2-9 Abort Command Timing

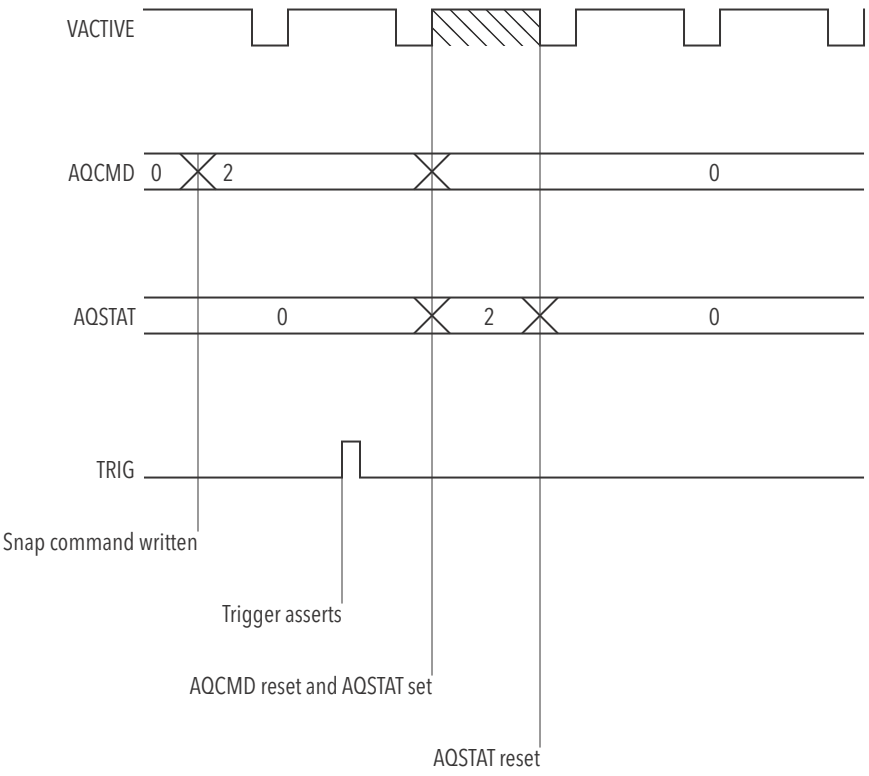

Figure 2-10 Snap Command Timing with ACQ_CON = 2

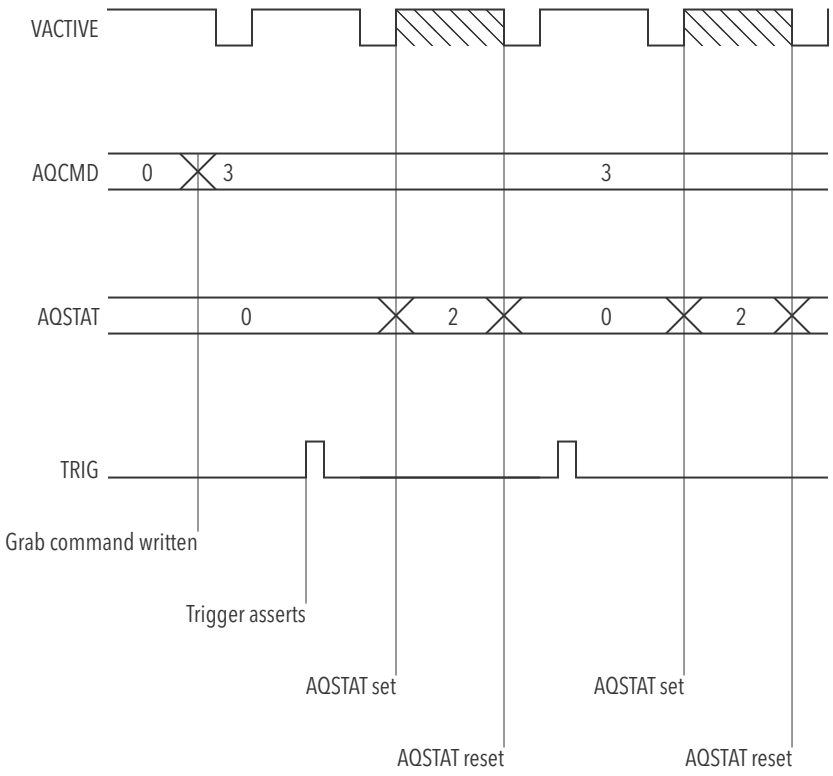

Figure 2-11 Grab Command Timing with ACQ_CON = 2

2.8 Trigger Processing

This section describes how the trigger circuit works. The trigger is used to initiate a vertical operation (for example, capturing one frame). There are three possible external hardware inputs to the trigger circuit and a software input. Assertion of the trigger can be delayed by up to 8192 lines (granularity is 8 lines). This delay works only with the external hardware trigger. Figure 2-12 illustrates the trigger circuit.

Note: The Alta only has one trigger input: TRIGGER_TTL.

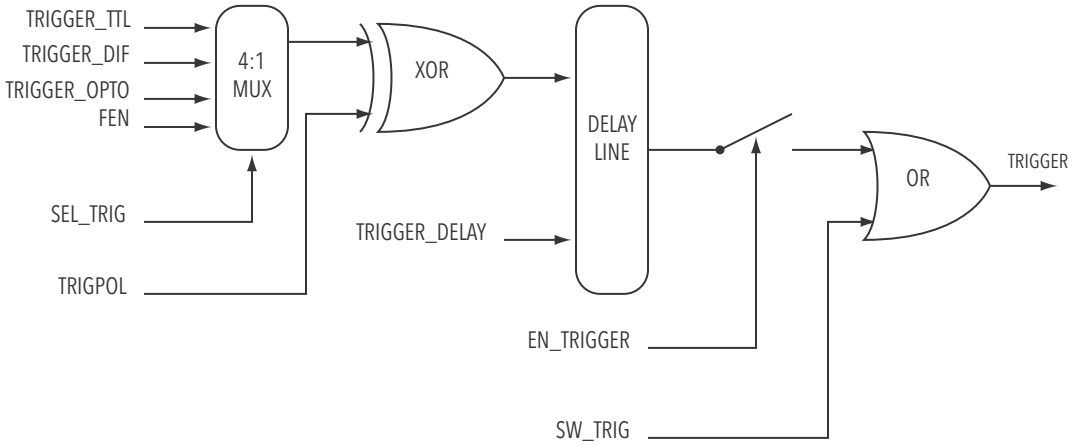

Figure 2-12 Trigger Circuit

2.9 Encoder Processing

This section describes how the encoder circuit works. The encoder is used to initiate a horizontal operation (for example, capturing one line). There are three possible external hardware inputs to the encoder circuit and a software input. The selected external encoder can be divided by the value in the ENC_DIV register. Figure 2-13 illustrates the encoder circuit.

Note: The Alta does not have any encoder inputs.

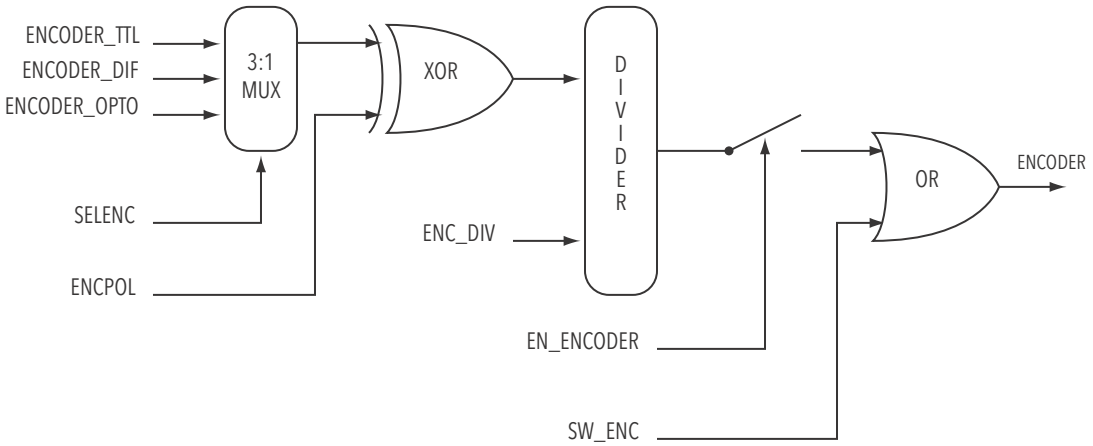

Figure 2-13 Encoder Circuit

2.10 The On-Board Signal Generator

The on-board signal generator has been replaced the New Timing Generator (NTG). Please see Section 3.1 for more information.

New Timing Generator

Chapter 3

3.1 Introduction

This section covers the new timing generator (NTG) which can control cameras connected to the Karbon-CL, Neon-CL and the Alta-AN. The purpose of this timing generator is to provide a simple system of controlling a camera's exposure time and line/frame rate from the frame grabber. The NTG is fully programmable and is easily controlled from software and/or from camera configuration files.

The NTG is based on a completely independent timing generator that is unrelated to acquisition and the CTabs. This timing generator is easy to program, is not depend on camera architecture or triggering modes, and offers the granularity and range that customers need. There is no connection between the NTG and the acquisition state machine, the CTabs, the VAW/HAW or the camera connected.

The New Timing Generator supports both triggered and free running modes. For triggered modes it supports both the trigger signal for area cameras or the encoder signal for line cameras.

The NTG requires that the camera be put in one of two modes. If the NTG is going to control just the line/frame rate, then the camera should be programmed into a "triggered" mode. In this case, the exposure is controlled by the camera. IF the NTG is to control both the line/frame rate as well as the exposure time, then the camera must be put into a "pulse width control" mode. In this case, neither the line/frame rate nor the exposure time are controlled by the camera. They are both completely controlled by the NTG.

Note: The NTG replaces the on-board timing generator that was prevouisly available on all boards. The NTG is much more flexible and easier to use. Please contact BitFlow if you have been using the previous on-board timing generator.

3.2 Components and Control

3.2.1 Periods and Frequencies

The NTG consists of a programmable signal generator based on a crystal controlled clock. This clock is always running and is unrelated to the camera connected or how other parts of the board are programmed. The base frequency of the clock is designed to handle any line scan camera system. For area scan cameras the clock can be divided 128 to increase the time range if very slow frame rates and/or line exposures are needed. To use the divided clock, program the bit NTG_TIME_MODE to 1. The frequency of the clock is different for the different frame grabber families as shown in Table 3-1.

Table 3-1 NTG Base Frequencies

Family	Base frequency	Reduced frequency
Karbon, Neon	7.3728 MHz	57.6000 KHz
Alta-AN	5 MHz	39.0625 KHz

The are two main timing registers: NTG_RATE, which controls the line/frame rate period, and NTG_EXPOSURE, which controls the exposure period. These are both 28 bits, which should be enough to support almost all applications. Table 3-2 shows the resulting ranges

Table 3-2 NTG Period Ranges

Family	Mode	Granularity (1 clock period)	Max Period
Karbon, Neon	Area	~17.4 microsecond	~77 minutes
	Line	~136 nanoseconds	~36 seconds
Alta-AN	Area	25.6 microseconds	~114 minutes
	Line	200 nanoseconds	~ 53 seconds

The NTG uses a counter internally to create the programmed waveforms. Because the NTG registers can be set for very long times, reprogramming the NTG can be time consuming. In order to speed up modifications to the NTG parameters, the register NTG_RESET can be used. Poke this bit to a 1 resets the NTG counter to zero, and starts a new cycle with the latest register values.

Note: Use the base frequency when a high resolotion timer is needed (fine granularity). Use the reduced frequency when long exposure periods and/or slow frame rates are needed (course granularity) You can use which ever mode suites your application regardless of whether you are using a line scan or an area scan camera..

3.2.2 Waveform polarity

There is also a register that inverts the waveform generated, NTG_INVERT. This is different than the old signal generator on the R64, which supports asserted-low signals by increasing the high time to be one-over-the-low time. The NTG system is much simpler, poke NTG_INVERT to a 1 and the waveform goes from asserted high to asserted low.

3.2.3 Triggering

The NTG has two modes of operation, free-running and one-shot mode. The bit that controls this mode is, NTG_ONESHOT. In free-run mode, both NTG_RATE and NTG_EXPOSURE are used. In one shot mode, only NTG_EXPOSURE is used, and the rate is controlled by the encoder/trigger.

Either the trigger input or the encoder input can be used to control the NTG in one-shot mode. This setting is controlled by the bit NTG_TRIG_MODE.

3.2.4 Output Signals

The waveform of the NTG can be routed to almost any of the board's output signals. The waveform can be send to the CC lines on the CL connector, or the GPOUT lines on the I/O connector. The CCx_CON bitfields can be used route the NTG signal to the CCs output. For example, program CC1_CON to 3 to get the NTG output on CC1. Similarly, the GPOUTx_CON bitfields can be used to route the NTG signals to the GPOUTx outputs. For example, to put the NTG output on GPOUT1, program GPOUT1_CON to 6. The NTG waveform can be sent simultaneously to any and all of these outputs.

3.2.5 Master/Slave Control

On boards that support more than one VFG (Karbon, Alta) there is the option to make the slave VFGs have the same timing as the master VFG, or to run each slave VFG's timing generator independently. The master VFGs always has its own timing. The selection is made by programming the NTG_SLAVE bit. On a given VFG, if this bit is set to 0, the VFG generates its own independent timing. If this bit is set to 1, the VFG's timing is the same as that of the master VFG.

Note: On multi-VFG boards, there is always a master and one or more slaves for programming purpose. The master VFG must always have the bit NTG_SLAVE set to 0. The slave VFGs can either be indpendent (NTG_SLAVE = 0) or the same as the master VFG (NTG_SLAVE = 1).

3.3 Timing

The following diagram illustrates all of the relevant parameters of the NTG.

Note: In the diagrams below NTG_INVERT is set to 0. If it were set to 1, these diagrams would be inverted.

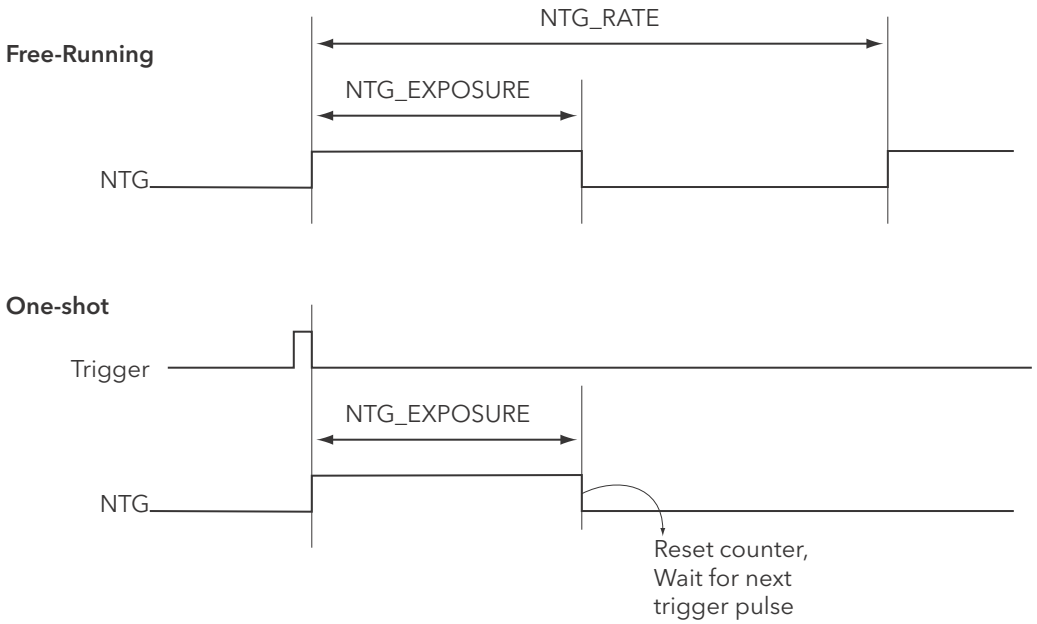

Figure 3-1 NTG Timing

In free running mode, the NTG counter will start at zero, one clock later it will assert the output. It will then count up to NTG_EXPOSURE clocks, then de-assert the output. It will then continue to count to NTG_EXPOSURE clocks then reset itself and start over.

In one-shot mode, the NTG clock will wait at zero and until the trigger is asserted, it will then start counting. On the first clock after the trigger is asserted it will assert its output. It will then count up to NTG_EXPOSURE clocks then de-assert its output. Next it will reset itself and wait for another trigger.

3.4 NTG Control Registers

The following table summarizes the registers:

Name	Locations	Purpose
NTG_RATE	CON17[27..0]	The line/frame rate period in units of one NTG clock (see Table 3-2 for values).
NTG_ONESHOT	CON17[30]	0 = Free-run mode, 1= one-shot mode, waits for either the trigger or the encoder pules (depending on NTR_TRIG_ MODE).
NTG_TRIG_MODE	CON17[31]	1 = Encoder for NTG trigger,0 = Trigger for NTG trigger
NTG_INVERT	CON18[30]	0 = NTG asserted high, 1 = NTG asserted low
NTG_TIME_MODE	CON18[31]	0 = Base NTG clock, 1= Base NTG clock / 128 (see Table 3-1 for values)
NTG_EXPOSURE	CON26[27..0]	The exposure time in units of one NTG clock.
NTG_RESET	CON26[30]	Writing a 1 resets the NTG counter
NTG_SLAVE	CON26[31]	0 = NTG master, 1 = NTG timing slaved to master

System Status

Chapter 4

4.1 Introduction

This chapter describes the system status report that the board supplies through its registers. The system status will help the users in setting up their system: the camera, the frame grabber, the cabling, the I/O and the software. The list of the status bits is given in the Table 4-1. If more information is available for a given specification there will be an entry in the column marked "Details". In addition, all of these registers are also described in Register Map chapter of this manual.

Table 4-1 Status Bits

Status Bits	Function and Relationship	Register	Details
AQSTAT	Acquisition status	CON3	Section 5.6
FACTIVE	Acquisition status, vertical active	CON3	Section 4.2
FCOUNT	Acquisition status, 3-bit frames counter	CON3	Section 4.2
LCOUNT	Camera status, LEN is toggling	CON4	Section 4.3
PCOUNT	Camera status, PCLK is toggling	CON4	Section 4.3
FENCOUNT	Camera status, FEN is toggling	CON4	Section 4.3
RD_TRIG_DIFF/TTL/OPTO	Trigger status	CON5	Section 4.4
RD_ENC_DIFF/TTL/OPTO	Encoder status	CON5	Section 4.4
TRIG_QUALIFIED	Selected trigger status	CON6	Section 4.5
VCOUNT	Acquisition status, VCTAB cycling	CON6	Section 4.6
HCOUNT	Acquisition status, HCTAB cycling	CON6	Section 4.6
LINES_TOGO	Acquisition status, current line in frame	CON19	Section 4.6
FIFO_EQ	Camera status, video value	CON20	Section 4.7
DEST_ADD	DMA running	CON22	Section 4.8

4.2 FACTIVE, FCOUNT

FACTIVE is 1 during the active vertical. It works for both area scan and line scan cameras. For both line scan and area scan cameras there is always a vertical size defined by ALPF.

FCOUNT is a 3-bit frame counter that is incremented by the rising edge of FACTIVE. It can be used to track acquisition, especially in triggered modes. FCOUNT works for both area scan and line scan cameras.

4.3 PCOUNT, LCOUNT, FENCOUNT

These three registers give an indication of the status the camera connected to the main connector:

PCOUNT is a 2-bit counter clocked by the camera's PCLK. Reading a constant value from this register indicates that the camera's clock does not reach the acquisition circuitry.

LCOUNT is a 2-bit counter clocked by the camera's LEN. Reading a constant value from this register indicates that the camera's LEN does not reach the acquisition circuitry.

FENCOUNT is a 2-bit counter clocked by the camera's FEN. Reading a constant value from this register indicates that the camera's FEN does not reach the acquisition circuitry.

4.4 RD_TRIG_DIFF/TTL/OPTO, RD_ENC_DIFF/TTL/OPTO

The level of all three trigger and all three encoder inputs can be read. This helps establish connection with external industrial equipment.

4.5 TRIG_QUALIFIED

The bit TRIG_QUALIFIED is the current active state of the current selected trigger. The trigger is selected by the SEL_TRIG register. Each individual input can be monitored via the corresponding RD_TRIG_XXX bit, but the TRIG_QUALIFIED always reports the state of the trigger input that is current being used by the acquisition circuitry.

4.6 VCOUNT, HCOUNT, LINES_TOGO

These three registers give feedback about the operation of the horizontal and vertical CTABs. VCOUNT is the address counter of the VCTAB. This register indicates the current VCTAB address.

HCOUNT is the 2 LSB of the HCTAB address counter. This register indicates only if the HCTAB is cycling. Reading a constant value on HCOUNT indicates that the HCTAB address is stuck.

LINES_TOGO specifies how more many lines there are till the end of the frame.

4.7 FIFO_EQ

This register gives the 8-bit value of the video from the first eight bits of the main connector. It is helpful to determine if the camera is reacting to light. Covering the camera's lens will yield a low value in this register. Pointing the camera to a light source will yield a high value in this register.

4.8 DEST_ADD

This register gives the DMA destination address. During acquisition, this register should change. Reading a constant value from this register suggests that the DMA operation is not progressing.

Camera Control Registers

Chapter 5

5.1 Introduction

This section enumerates all of the bitfields in all of the registers used to control the acquisition and external I/O. If you compare the Alta, Karbon, Neon and R64 manuals you will see that almost all of these registers are the same. There are only a few bits that are different between these two models, these will be indicated in the bitfield definitions. Registers that are related to DMA operations, which are different between the Alta, Neon, R64 and the Karbon families, have their own chapters.

All of the registers are 32 bits wide. These wide registers are named CON0, CON1, etc. Each registers is broken into one or more bitfields. Bitfields can be from one to 32 bits wide. Each bitfield controls a specific function on the board.

5.2 Bitfield definitions

5.2.1 Example Bitfield Definition

Here is what each bitfield definition looks like:

BITFIELD R/W, CON0[7..0], Alta, Karbon, Neon, R64

BitField discussion.

5.2.2 Bitfield Definition Explanation.

The definitions is broken into three sections (see Table 5-1).

Table 5-1 Bitfield Sections.

Section	Meaning
Bitfield name	This is the name of the bitfield. This name is use to program this bitfield from software or from within and camera configuration file. When programming bitfields from software using a Peek or Poke function, the bitfield is preceded with "REG_". For example the bitfield CFREQ is referred to in software as REG_CFREQ.
Bitfield details	This section describes how the bitfield is accessed. The first part describes the how the bits can be accessed. For example R/W means the register can be both read and writen. See theTable 5-2 for details.The second part is the wide register that the bitfield is located in. In the example above this bitfield is in CON0. Following the wide register name is a bitfield location description, in hardware engineering format. For example, [7..0], means the bitfield has 8 bits, location in positions 0 to 7. Finally this section also indicates if the register is specific to only one product family.
Bitfield discussion	This section explains the purposed of the bitfield in detail. Usually meaning of every possible value of the bitfield is listed.

Table 5-2 explains the abbreviations used in the bitfield definitions.

Table 5-2 Abbreviations

Access	Meaning
R/W	Bitfield can be read and written.
RO	Bitfield can only be read. Writing to this bit has no effect.
WO	Bitfield can only be written. Reading from this bit will return meaningless values.
Karbon	This bitfield is functional on the Karbon.
Neon	This bitfield is functional on the Neon
R64	This bitfield is functional on the R64 family.
Alta	This bitfield is functional on the Alta family.

5.3 CON0 Register

Bit	Name
0	CFGDATA
1	CFGSTATUS
2	CFGEN
3	CFGDONE
4	CFGCLOCK
5	FW_7MHZ
6	Reserved
7	POCL_EN
8	CFREQ
9	CFREQ
10	CFREQ
11	Reserved
12	L_CLKCON
13	L_CLKCON
14	SEL_UCLKC_7MHZ
15	RELOAD_FPGA
16	FW_SEL
17	FW_SEL
18	FW_SEL
19	CPLD_MODE
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

CFGDATA R/W, CON0[0], R64

Used for downloading firmware.

CFGSTATUS R/W, CON0[1], R64

Used for downloading firmware.

CFGEN R/W, CON0[2], R64

Used for downloading firmware.

CFGDONE R/W, CON0[3], R64

Used for downloading firmware.

CFGCLOCK R/W, CON0[4], R64

Used for downloading firmware.

FW_7MHZ RO, CON0[5], Alta, Karbon, Neon, R64

If this bit is set, then the board has the update Firmware which can program the frequency of the UART clock to 7.3 MHz. If this bit is zero, then the board has the original firmware and the UART can only be driver by an 8 MHz clock. See also the bit: SEL_UCLK_7MHz.

POCL_EN R/W, CON0[7], Neon

This bit turns the PoCL Safe Power system. This bit must be set to one in order to enable power to PoCL cameras. However, the system uses the Safe Power system, so a number of conditions must be met before power is actually applied to the camera.

CFREQ R/W, CON0[10..8], Alta, Karbon, Neon, R64

These bits control the frequency of the CLOCK generated on-board.

CFREQ	Frequency
0 (000b)	DC
1 (001b)	3.75 MHz
2 (010b)	7.5 MHz
3 (011b)	15 MHz
4 (100b)	24 MHz
5 (101b)	30 MHz
6 (110b)	48 MHz
7 (111b)	60 MHz

L_CLKCON R/W, CON0[13..12], Alta, Karbon, Neon, R64

These bits control the local bus clock frequency. For normal operation, this register should always be set for 0. The other codes are for test/diagnostics.

L_CLKCON	Frequency
0 (000b)	60 MHz
1 (001b)	48 MHz
2 (010b)	24 MHz
3 (011b)	Reserved

SEL_UCLK_7MHZ R/W, CON0[14], Alta, Karbon, Neon, R64

This bit selects the frequency that is used to driver the UART for serial communications. This functionality is only available on boards with update firmware. The bit FW_7MHZ can be used to check the version of the firmware.

SEL_UCLK_7MHZ	Frequency
0	8 MHz
1	7.3 MHz

RELOAD_FPGA WO, CON0[15], Karbon, Neon

Writing to this bit causes the FGPA to be reloaded from Flash memory. This bit should only be accessed from the driver as the PCI Configuration space is overwritten by this operation. This is not a user programmable bit.

FW_SEL R/W, CON0[18..16], Alta, Karbon, Neon, R64

These bits are used to select different modes for a given type of firmware. For each major type of CCD tap configuration, there is a separate firmware file that is downloaded to the board. However, in some cases different manufacturers chose slightly different ways to implement the same tap configuration. In these cases this bitfield is used to select between the different modes. As the meaning for this bitfield differ for each firmware file, and these bits are rarely used, the specific definitions of this bitfield are not enumerated here.

CPLD_MODE R/W, CON0[19], Neon

On the Neon, the CPLD used to load the FPGAs has two modes. This bit is used to set the mode. This is not a user programmable bit.

5.4 CON1 Register

Bit	Name
0	VCNT_RLS_ZERO
1	VCNT_RLS_ZERO
2	VCNT_RLS_ZERO
3	VCNT_RST
4	VCNT_RST
5	VCNT_RST
6	VCNT_LD
7	VCNT_LD
8	VCNT_LD
9	VCNT_RLS_STK
10	VCNT_RLS_STK
11	VCNT_RLS_STK
12	ABORT_CON
13	ABORT_CON
14	ABORT_CON
15	NO_VB_WAIT
16	ACQ_CON
17	ACQ_CON
18	ACQ_CON
19	FREEZE_CON
20	FREEZE_CON
21	FREEZE_CON
22	ACQ_SAFETY
23	NO_RULE
24	INT_CTAB
25	INT_OVSTEP
26	INT_HW
27	INT_TRIG
28	INT_SER
29	INT_QUAD
30	INT_TRIGCON
31	INT_TRIGCON

VCNT_RLS_ZERO R/W, CON1[2..0], Alta, Karbon, Neon, R64

This register controls how the Vertical CTAB counter (VCOUNT) is released from zero.

VCNT_RLS_ZERO	Meaning
0 (000b)	Normal operation. VCOUNT does not stick at zero.
1 (001b)	Edge Mode - VCOUNT sticks at zero. VCOUNT is released from zero by the leading edge of the trigger.
2 (010b)	Level Mode - VCOUNT sticks at zero only if the trigger is de-asserted. If trigger is asserted, then VCOUNT does not stick at zero. VCOUNT is released from zero by the leading edge of trigger.
3 (011b)	Reserved.

VCNT_RST R/W, CON1[5..3], Alta, Karbon, Neon, R64

This register controls how the Vertical CTAB counter (VCOUNT) is reset to zero. In all modes the VCOUNT will also be reset by any of the following four signals/events:

The SW_RESET
The ABORT command
The RST_HVCOUNT bit in CON4
VCOUNT reaching a 1 in the VRESET CTAB

VCNT_RST	Meaning
0 (000b)	VCOUNT is reset by the End of Vertical Acquisition Window or by the VRESET column in the VCTAB.
1 (001b)	VCOUNT is reset by the de-assertion of the trigger (triggered termination) or the end of VAW or by the VRESET column in the VCTAB.
2 (010b)	VCOUNT is reset by the VRESET column in the VCTAB.
3 (011b)	VCOUNT is reset by the assertion of FEN or by the VRESET column in the VCTAB.
4 (100b)	VCOUNT is reset by the de-assertion of the trigger, or by the VRESET column in the VCTAB.

VCNT_LD R/W, CON1[8..6], Alta, Karbon, Neon, R64

This registers controls how the Vertical CTAB counter (VCOUNT) is loaded with the 8000h value.

VCNT_LD	Meaning
0 (000b)	No load operation performed.
1 (001b)	VCOUNT is loaded at the assertion of FEN qualified with the ENVLOAD column in the VCTAB.
2 (010b)	VCOUNT is loaded at the assertion of FEN.
3 (011b)	VCOUNT is loaded at the assertion of trigger.

VCNT_RLS_STK R/W, CON1[11..9], Alta, Karbon, Neon, R64

This register controls the stick/release of the VCOUNT to/from address 7ff0h.

VCNT_RLS_STK	Meaning
0	VCOUNT does not stick at 7FF0h.
1	VCOUNT sticks at 7FF0h. It will be released from that address by a LOAD or RESET operation.

ABORT_CON R/W, CON1[14..12], Alta, Karbon, Neon, R64

This register controls the ABORT operation of the Acquisition State Machine.

ABORT_CON	Meaning
0	Acquisition will be aborted by a host command.
1	Acquisition will be aborted by de-assertion of trigger of by a host ABORT command.

NO_VB_WAIT R/W, CON1[15], Alta, Karbon, Neon, R64

This bit has the following properties.

NO_VB_WAIT	Meaning
0	Wait for the Vertical Active Window before executing the Head Tag Quad.
1	Do not wait for the Vertical Active Window for executing the Head Tag Quad.

ACQ_CON R/W, CON1[18..16], Alta, Karbon, Neon, R64

This register controls the execution of the acquisition command.

ACQ_CON	Meaning
0 (000b)	Acquisition is initiated by host writing the command.
1 (001b)	The acquisition command written by host will start executing at assertion of trigger (triggered acquisition). Only the SNAP and GRAB commands require a trigger to be latched. The FREEZE command will work normally.
2 (010b)	While the GRAB command is on, a frame will be acquired at the assertion of trigger.
3 (011b)	Continuous acquisition mode. Host commands are ignored. Data will be acquired continuously as long as the TRIGGER is asserted.
4 (100b)	A GRAB command will be issued every time the TRIGGER asserts. The GRAB can be terminated after a programmable number of frames by using the AQ_COUNT register. This mode initiated by manually issuing a GRAB command, and terminated after manually issuing a FREEZE. The AQ_STAT register will return GRAB mode as long as the board is in this mode, regardless of whether the board is actually grabbing or not.

FREEZE_CON R/W, CON1[21..19], Alta, Karbon, Neon, R64

This register controls the FREEZE operation.

FREEZE_CON	Meaning
0 (000b)	FREEZE initiated by host command.
1 (001b)	FREEZE initiated by the Acquisition Counter or by the host command.
2 (010b)	FREEZE initiated by the de-assertion of trigger or by the host command.

ACQ_SAFETY R/W, CON1[22], Alta, Karbon, Neon, R64

Future use

NO_RULE R/W, CON1[23], R64

Test/diagnostic bit. For normal operation this bit should always be set to 0. When set to 1, the DMA engine will DMA data at maximum speed, regardless of wether the data is valid.

INT_CTAB R/W, CON1[24], Alta, Karbon, Neon, R64

This interrupt will be set by the interrupt bit in the VCTAB or by the host writing to this bit. The interrupt will be enabled if its corresponding mask, ENINT_CTAB, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 1.

INT_CTAB	Meaning
0	No interrupt from CTAB
1	Interrupt from CTAB asserted.

INT_OVSTEP R/W, CON1[25], Alta, Karbon, Neon, R64

This interrupt will be set if an overflow occurred in the FIFO or by the host writing to this bit. The interrupt will be enabled if its corresponding mask, ENINT_OVSTP, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 2.

INT_OVSTP	Meaning
0	No interrupt from overflow
1	Interrupt from overflow asserted.

INT_HW R/W, CON1[26], Alta, Karbon, Neon, R64

This interrupt will be set by a hardware exception, a loss of sync or by the host writing to this bit. The interrupt will be enabled if its corresponding mask, ENINT_HW, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 3.

INT_HW	Meaning
0	No interrupt from HW
1	Interrupt from HW asserted.

INT_TRIG R/W, CON1[27], Alta, Karbon, Neon, R64

This interrupt will be set by a trigger edge or by the host writing to this bit (see register INT_TRIGCON below). The interrupt will be enabled if its corresponding mask, ENINT_TRIG, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 4.

INT_TRIG	Meaning
0	No interrupt from trigger
1	Interrupt from trigger asserted.

INT_SER RO, CON1[18], Alta, Karbon, Neon, R64

This interrupt will be set by the on board UART that implements the serial communication protocol. The interrupt will be enabled if its corresponding mask, ENINT_SER, has been set to 1. This interrupt can be cleared by the host writing to the UART.

INT_SER	Meaning
0	No interrupt from UART
1	Interrupt from UART asserted.

INT_QUAD R/W, CON1[29], Alta, Karbon, Neon, R64

This interrupt will be set by a DMA QUAD or by the host writing to this bit. The interrupt will be enabled if its corresponding mask, ENINT_QUAD, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 5.

INT_QUAD	Meaning
0	No interrupt from QUAD
1	Interrupt from QUAD asserted.

INT_TRIGCON R/W, CON1[31..20], Alta, Karbon, Neon, R64

This register controls the trigger edge that will cause an interrupt:

INT_TRIGCON	Meaning
0 (00b)	reserved
1 (01b)	Assert interrupt on rising edge of trigger.
2 (10b)	Assert interrupt on falling edge of trigger.
3 (11b)	Assert interrupt on both the rising and the falling edge of the trigger.

5.5 CON2 Register

Bit	Name
0	HCNT_RLS_ZERO
1	HCNT_RLS_ZERO
2	HCNT_RLS_ZERO
3	HCNT_RST
4	HCNT_RST
5	HCNT_RST
6	HCNT_LD
7	HCNT_LD
8	HCNT_LD
9	HCNT_RLS_STK
10	HCNT_RLS_STK
11	HCNT_RLS_STK
12	RST_HVCOUNT
13	RST_DPM_ADDR
14	CTABHOLD
15	Reserved
16	CC1_CON
17	CC1_CON
18	CC1_CON
19	CC2_CON
20	CC2_CON
21	CC2_CON
22	CC3_CON
23	CC3_CON
24	CC3_CON
25	CC4_CON
26	CC4_CON
27	CC4_CON
28	CMDWRITE
29	CMDWRITE
30	CMDWRITE
31	QTBSRC

HCNT_RLS_ZERO R/W, CON2[2..0], Alta, Karbon, Neon, R64

This register controls the release of the HCOUNT from zero.

HCNT_RLS_ZERO	Meaning
0	HCOUNT does not stop at 000h.
1	HCOUNT stops at 000h. It will be released by the assertion of the encoder.

HCNT_RST R/W, CON2[5..3], Alta, Karbon, Neon, R64

This register controls the reset of the HCOUNT. In all cases, the HCOUNT will also be reset by any of the following functions:

SW_RESET
RST_HVCOUNT
ABORT command.

HCNT_RST	Meaning
0 (000b)	HCOUNT will be reset by the end of the Horizontal Active Window.
1 (001b)	HCOUNT will be reset by the assertion of FEN or the HRESET from the HCTAB.
2 (010b)	HCOUNT will be reset by the HRESET in the HCTAB.

HCNT_LD R/W, CON2[8..6], Alta, Karbon, Neon, R64

This register controls the loading of the HCOUNT with 2000h.

HCNT_LD	Meaning
0 (000b)	HCOUNT will not be loaded.
1 (001b)	HCOUNT will be loaded by assertion of LEN if the ENHLOAD function in the HCTAB is set to 1.
2 (010b)	HCOUNT will be loaded by assertion of encoder if the ENHLOAD function in the HCTAB is set to 1.

HCNT_RLS_STK R/W, CON2[11..9], Alta, Karbon, Neon, R64

This register controls the HCOUNT sticking at 1FF0h.

HCNT_RLS_STK	Meaning
0	HCOUNT will not stick at 1FF0h.
1	HCOUNT will stick at 1FF0h. It will be released by a load or reset command.

RST_HVCOUNT WO, CON2[12], Alta, Karbon, Neon, R64

This bit has the following properties.

RST_HVCOUNT	Meaning
0	Normal operation for HCOUNT, VCOUNT
1	Reset HCOUNT, VCOUNT..

RST_DPM_ADDR WO, CON2[13], Alta, Karbon, Neon, R64

This bit has the following properties.

RST_DPM_ADDR	Meaning
0	Normal operation for DPM_ADDR
1	Reset DPM_ADDR..

CTABHOLD R/W, CON2[14], Alta, Karbon, Neon, R64

This bit has the following properties.

CTABHOLD	Meaning
0	Normal operation for CTABs
1	Freeze outputs and operation of CTABs..

CCI_CON R/W, CON2[18..16], Alta, Karbon, Neon, R64

This register selects the signal steered to the CC1.

CC1_CON	Signal steered to CC1
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running signal generated on-board
4 (100b)	Trigger input
5 (101b)	GPIN0
6 (110b)	0
7 (111b)	1

CC2_CON R/W, CON2[21..19], Alta, Karbon, Neon, R64

This register selects the signal steered to the CC2.

CC2_CON	Signal steered to CC2
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running signal generated on-board
4 (100b)	Trigger Input
5 (101b)	GPIN0
6 (110b)	0
7 (111b)	1

CC3_CON R/W, CON2[24..22], Alta, Karbon, Neon, R64

This register selects the signal steered to the CC3.

CC3_CON	Signal steered to CC3
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running signal generated on-board
4 (100b)	Trigger input
5 (101b)	GPIN0
6 (110b)	0
7 (111b)	1

CC4_CON R/W, CON2[27..25], Alta, Karbon, Neon, R64

This register selects the signal steered to the CC4. Note that this CC control is slightly different than the previous three. CC4 can be controlled by CT3. This changes allows all four CTs to be tied to a CC.

CC4_CON	Signal steered to CC4
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running signal generated on-board
4 (100b)	Trigger input
5 (101b)	CT3 from CTAB
6 (110b)	0
7 (111b)	1

CMDWRITE R/W, CON2[30..28], Alta, Karbon, Neon, R64

This registers selects the interrupt bit to be modified by the host. While an interrupt's code is set, that interrupt can not be asserted by its source. It can be modified only by the host. This mechanism allows to perform reliable read-modify-write cycles.

CMDWRITE	Interrupt allowed for host access
0 (000b)	No interrupt can be accessed by host
1 (001b)	INT_CTAB
2 (010b)	INT_OVSTP
3 (011b)	INT_HW
4 (100b)	INT_TRIG
5 (101b)	INT_QTAB
6 (110b)	INT_EOF
7 (111b)	reserved

QTBSRC RO, CON2[31], Alta, Karbon, Neon, R64

Always read back 1.

5.6 CON3 Register

Bit	Name
0	AQCMD
1	AQCMD
2	AQSTAT
3	AQSTAT
4	FACTIVE
5	FCOUNT
6	FCOUNT
7	FCOUNT
8	REV_DCC
9	REV_DCC
10	REV_DCC
11	REV_DCC
12	REV_DCC
13	REV_DCC
14	REV_DCC
15	REV_DCC
16	REV_DCC
17	REV_DCC
18	REV_DCC
19	REV_DCC
20	REV_DCC
21	REV_DCC
22	REV_DCC
23	REV_DCC
24	AUX_DETECT
25	GPIN0
26	GPIN1
27	GPIN2
28	GPIN3
29	GPIN4
30	SW
31	SW

AQCMD R/W, CON3[1..0], Alta, Karbon, Neon, R64

This register is the acquisition command to be executed in the next frame.

AQCMD	Meaning
0 (00b)	FREEZE
1 (01b)	ABORT
2 (10b)	SNAP
3 (11b)	GRAB

AQSTAT RO, CON3[3..2], Alta, Karbon, Neon, R64

The AQSTAT register describes the acquisition command currently being executed.

AQSTAT	Meaning
0 (00b)	FREEZE
1 (01b)	ABORT
2 (10b)	SNAP
3 (11b)	GRAB

FACTIVE RO, CON3[4], Alta, Karbon, Neon, R64

FACTIVE	Meaning
0	Camera outside the Vertical Acquisition Window
1	Camera within the Vertical Acquisition Window

FCOUNT RO, CON3[7..5], Alta, Karbon, Neon, R64

This is a 3-bit modulo-8 counter. The counter is incremented by the start of the Vertical Acquisition Window. It is used as a debug/diagnostic tool.

REV_DCC WO, CON3[23..8], Alta, Karbon, Neon, R64

FW revision.

AUX_DETECT RO, CON3[24], Karbon

This bit is set to a one if the Karbon auxiliary board is attached.

GPIN0 RO, CON3[25], Alta, Karbon, Neon, R64

Controlled by inputs on the IO connector. The logical value applied to the corresponding pin will be reflected in this register. See also Section 10.4 for interfacing information.

GPIN1 RO, CON3[26], Alta, Karbon, Neon, R64

Controlled by inputs on the IO connector. The logical value applied to the corresponding pin will be reflected in this register. See also Section 10.4 for interfacing information.

GPIN2 RO, CON3[27], Alta, Karbon, Neon, R64

Controlled by inputs on the IO connector. The logical value applied to the corresponding pin will be reflected in this register. See also Section 10.4 for interfacing information.

GPIN3 RO, CON3[28], Alta, Karbon, Neon, R64

Controlled by inputs on the IO connector. The logical value applied to the corresponding pin will be reflected in this register. See also Section 10.4 for interfacing information.

GPIN4 RO, CON3[29], Alta, Karbon, Neon, R64

Controlled by inputs on the IO connector. The logical value applied to the corresponding pin will be reflected in this register. See also Section 10.4 for interfacing information.

SW RO, CON3[31..30], Alta, Karbon, Neon, R64

Controlled by inputs on the IO connector. The logical value applied to the corresponding pin will be reflected in this register. See also Section 10.4 for interfacing information.

5.7 CON4 Register

Bit	Name
0	ENINT_CTAB
1	ENINT_OVSTEP
2	ENINT_HW
3	ENINT_TRIG
4	ENINT_SER
5	ENINT_QUAD
6	EOF_IN_AQ
7	INT_ANY
8	ENINT_ALL
9	AUX_CAM
10	GPOUT0
11	GPOUT1
12	GPOUT2
13	GPOUT3
14	GPOUT4
15	GPOUT5
16	GPOUT6
17	RST_SER
18	OVS
19	RST_OVS
20	CL_DISABLE
21	LCOUNT
22	LCOUNT
23	PCOUNT
24	PCOUNT
25	FENCOUNT
26	FENCOUNT
27	POP_TOSS
28	PUMP_OFF
29	DMA_BUSY
30	HAW_START
31	VAW_START

ENINT_CTAB R/W, CON4[0], Alta, Karbon, Neon, R64

This bit has the following properties.

ENINT_CTAB	Meaning
0	CTAB interrupt disabled
1	CATB interrupt enabled

ENINT_OVSTEP R/W, CON4[1], Alta, Karbon, Neon, R64

This bit has the following properties.

ENINT_OVSTEP	Meaning
0	OVERSTEP interrupt disabled
1	OVERSTEP interrupt enabled

ENINT_HW R/W, CON4[2], Alta, Karbon, Neon, R64

This bit has the following properties.

ENINT_HW	Meaning
0	HW interrupt disabled
1	HW interrupt enabled

ENINT_TRIG R/W, CON4[3], Alta, Karbon, Neon, R64

This bit has the following properties.

ENINT_TRIG	Meaning
0	Trigger interrupt disabled
1	Trigger interrupt enabled

ENINT_SER R/W, CON4[4], Alta, Karbon, Neon, R64

This bit has the following properties.

ENINT_SER	Meaning
0	UART interrupt disabled
1	UART interrupt enabled

ENINT_QUAD R/W, CON4[5], Alta, Karbon, Neon, R64

This bit has the following properties.

ENINT_QUAD	Meaning
0	QUAD interrupt disabled
1	QUAD interrupt enabled

EOF_IN_AQ R/W, CON4[6], Alta, Karbon, Neon, R64

This bit enables gating the INT_EOF interrupt with acquisition. This functionality makes it easier to write software that relies on the INT_EOF interrupt. Without this functionality, the INT_EOF interrupt would occur continuously based on the camera or trigger's timing, even if the board is not currently acquiring. In this case, the software will have to flush these interrupts out of the queue before starting acquisition. With this functionality enable, interrupts only occur during acquisition..

EOF_IN_AQ	Meaning
0	INT_EOF interrupt will be asserted unconditionally at the end of the frame.
1	INT_EOF interrupt will be asserted at the end of the frame only if the board is acquiring, i.e. only during SNAP/GRAB states.

INT_ANY RO, CON4[7], Alta, Karbon, Neon

On the products that use the PLDA engine, this bit indicates that an interrupt was emitted by the board. This bit can be checked first to see if some event caused the interrupt, before inquiring other bits to see the actual cause of the interrupt.

ENINT_ALL R/W, CON4[8], Alta, Karbon, Neon

This bit enables or disables all interrupts on boards that use the PLDA engine.

AUX_CAM R/W, CON4[8], R64

Future use.

GPOUT0 R/W, CON4[10], Alta, Karbon, Neon, R64

The value written in this register will be reflected on the IO connector. See also CON8 for signals steered to the GPOUTs and Section 10.5 for electrical interfacing.

GPOUT1 R/W, CON4[11], Alta, Karbon, Neon, R64

The value written in this register will be reflected on the IO connector. See also CON8 for signals steered to the GPOUTs and Section 10.5 for electrical interfacing.

GPOUT2 R/W, CON4[12], Alta, Karbon, Neon, R64

The value written in this register will be reflected on the IO connector. See also CON8 for signals steered to the GPOUTs and Section 10.5 for electrical interfacing.

GPOUT3 R/W, CON4[13], Alta, Karbon, Neon, R64

The value written in this register will be reflected on the IO connector. See also CON8 for signals steered to the GPOUTs and Section 10.5 for electrical interfacing.

GPOUT4 R/W, CON4[14], Alta, Karbon, Neon, R64

The value written in this register will be reflected on the IO connector. See also CON8 for signals steered to the GPOUTs and Section 10.5 for electrical interfacing.

GPOUT5 R/W, CON4[15], Alta, Karbon, Neon, R64

The value written in this register will be reflected on the IO connector. See also CON8 for signals steered to the GPOUTs and Section 10.5 for electrical interfacing.

GPOUT6 R/W, CON4[16], Alta, Karbon, Neon, R64

The value written in this register will be reflected on the IO connector. See also CON8 for signals steered to the GPOUTs and Section 10.5 for electrical interfacing.

RST_SER R/W, CON4[17], Alta, Karbon, Neon, R64

This bit has the following properties.

RST_SER	Meaning
0	UART normal operation
1	UART's reset line asserted

OVS RO, CON4[18], Alta, Karbon, Neon, R64

This is a latched overstep bit.

OVS	Meaning
0	No overstep occurred since this bit was cleared
1	At least one overstep occurred since this bit was cleared

RST_OVS R/W, CON4[19], Alta, Karbon, Neon, R64

This bit has the following properties.

RST_OVS	Meaning
0	OVS bit in normal operation
1	OVS bit is reset

CL_DISABLE R/W, CON4[20], Alta, Karbon, Neon, R64

This bit enables/disables the CL chips; used for diagnostics. For normal operation this bit should always be set to 0.

CL_DISABLE	Meaning
0	All CL receivers are enabled.
1	All CL receivers are disabled.

LCOUNT RO, CON4[22..21], Alta, Karbon, Neon, R64

This is a 2-bit counter clocked by the LEN supplied by the Camera Link main connector. Reading this counter and observing changes between reads indicates an active LEN.

PCOUNT RO, CON4[24..23], Alta, Karbon, Neon, R64

This is a 2-bit counter clocked by the PCLK supplied by the Camera Link main connector. Reading this counter and observing changes between reads indicates an active PCLK.

FENCOUNT RO, CON4[26..25], Alta, Karbon, Neon, R64

This is a 2-bit counter clocked by the FEN supplied by the Camera Link main connector. Reading this counter and observing changes between reads indicates an active FEN.

POP_TOSS R/W, CON4[27], R64, Alta, Karbon, Neon, R64

For normal operation this bit should be set to 0. It is used for high-level clean-up.

POP_TOSS	Meaning
0	DMA engine's normal operation.
1	DMA engine flushes the receive FIFO without executing any QUADs.

PUMP_OFF R/W, CON4[28], R64, Alta, Karbon, Neon, R64

For normal operation this bit should be set to 0. It is used for high-level clean-up.

PUMP_OFF	Meaning
0	DMA engine's normal operation.
1	Inhibit DMA operation.

DMA_BUSY RO, CON4[29], R64, Alta, Karbon, Neon, R64

This bit indicates the state of the DMA engine.

DMA_BUYS	Meaning
0	DMA engine is idle.
1	DMA engine is currently DMAing data.

HAW_START R/W, CON4[30], Alta, Karbon, Neon, R64

This bit has the following properties.

HAW_START	Meaning
0	The start of the Horizontal Active Window (HAW) is controlled by the start of the LEN.
1	The start of the Horizontal Active Window is controlled by the HSTART column in the HCTAB.

VAW_START R/W, CON4[31], Alta, Karbon, Neon, R64

This bit has the following properties.

VAW_START	Meaning
0	The start of the Vertical Active Window (VAW) is controlled by the start of the FEN.
1	The start of the Vertical Active Window is controlled by the VSTART column in the VCTAB.

5.8 CON5 Register

Bit	Name
0	SEL_TRIG
1	SEL_TRIG
2	TRIGPOL
3	SW_TRIG
4	SELENC
5	SELENC
6	ENCPOL
7	SW_ENC
8	RD_TRIG_DIFF
9	RD_TRIG_TTL
10	RD_TRIG_OPTO
11	RD_ENC_DIFF
12	RD_ENC_TTL
13	RD_ENC_OPTO
14	TRIGGER_DELAY
15	TRIGGER_DELAY
16	TRIGGER_DELAY
17	TRIGGER_DELAY
18	TRIGGER_DELAY
19	TRIGGER_DELAY
20	TRIGGER_DELAY
21	TRIGGER_DELAY
22	TRIGGER_DELAY
23	TRIGGER_DELAY
24	ENINT_EOF
25	INT_EOF
26	RD_FEN
27	CCSYNC
28	CCSYNC
29	CCSYNC
30	EN_TRIGGER
31	EN_ENCODER

SEL_TRIG R/W, CON5[1..0], Alta, Karbon, Neon, R64

Controls the source of the internal trigger signal.

SEL_TRIG	Meaning
0 (00b)	The trigger used by the board is the differential trigger on the IO connector.
1 (01b)	The trigger used by the board is the TTL trigger on the IO connector.
2 (10b)	The trigger used by the board is the opto-coupled trigger on the IO connector.
3 (11b)	The FEN signal on the CL1 connector will be used as trigger. When this mode is used, the register FENPOL is used to control the polarity of the trigger signal.

TRIGPOL R/W, CON5[2], Alta, Karbon, Neon, R64

This bit has the following properties.

TRIGPOL	Meaning
0	Trigger is asserted on the rising edge.
1	Trigger is asserted on the falling edge.

SW_TRIG R/W, CON5[3], Alta, Karbon, Neon, R64

The SW trigger is OR-ed with the external trigger. The polarity of the SW trigger is always active-HI. TRIGPOL has no effect on the SW trigger.

SW_TRIG	Meaning
0	SW trigger de-asserted.
1	SW trigger asserted.

SELENC R/W, CON5[5..4], Alta, Karbon, Neon, R64

This bitfield has the following properties.

SELENC	Meaning
0 (00b)	The encoder used by the board is the differential encoder on the IO connector.
1 (01b)	The encoder used by the board is the TTL encoder on the IO connector.
2 (10b)	The encoder used by the board is the opto-coupled encoder on the IO connector.
3 (11b)	Reserved

ENCPOL R/W, CON5[6], Alta, Karbon, Neon, R64

This bitfield has the following properties.

ENCPOL	Meaning
0	Encoder is asserted on rising edge.
1	Encoder is asserted on falling edge.

SW_ENC R/W, CON5[7], Alta, Karbon, Neon, R64

The SW encoder is OR-ed with the external encoder. The polarity of the SW encoder is always active-HI. ENCPOL has no effect on the SW encoder

SW_ENC	Meaning
0	SW encoder de-asserted.
1	SW encoder asserted.

RD_TRIG_DIFF RO, CON5[8], Alta, Karbon, Neon, R64

This register reflects the status of the differential trigger input on the IO connector, pins 1,2.

RD_TRIG_TTL RO, CON5[9], Alta, Karbon, Neon, R64

This register reflects the status of the TTL trigger input on the IO connector, pin 3.

RD_TRIG_OPTO RO, CON5[10], Alta, Karbon, Neon, R64

This register reflects the status of the opto-coupled trigger input on the IO connector, pins 4,5.

RD_ENC_DIFF RO, CON5[11], Alta, Karbon, Neon, R64

This register reflects the status of the differential encoder input on the IO connector, pins 7,8.

RD_ENC_TTL RO, CON5[12], Alta, Karbon, Neon, R64

This register reflects the status of the TTL encoder input on the IO connector, pin 9

RD_ENC_OPTO RO, CON5[13], Alta, Karbon, Neon, R64

This register reflects the status of the opto-coupled encoder input on the IO connector, pins 10, 11.

TRIGGER_DELAY R/W, CON5[23..14], Alta, Karbon, Neon, R64

The number N written in this register will delay the trigger by 8N lines.

ENINT_EOF R/W, CON4[24], Alta, Karbon, Neon, R64

This bitfield has the following properties.

ENINT_EOF	Meaning
0	End of frame interrupt disabled.
1	End of frame interrupt enabled.

INT_EOF R/W, CON4[25], Alta, Karbon, Neon, R64

This interrupt will be set by the acquisition state machine at the end of the frame (end of VAW). This ordinarily corresponds to the camera's end of frame. However, if the board is in start-stop triggered mode, this interrupt with also occur when the trigger de-asserts. The host writing a 1 to this bit will also cause and interrupt. The interrupt

will be enabled if its corresponding mask, ENINT_EOF, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 6.

INT_TRIG	Meaning
0	No interrupt from end of frame.
1	Interrupt from end of frame.

RD_FEN RO, CON5[26], Alta, Karbon, Neon, R64

This register reflects the status of the FEN signal on the CL1 connector.

CC_SYNC R/W, CON5[29..26], Alta, Karbon, Neon, R64

This register controls how the CC outputs are synchronized.

CCSYNC	Meaning
0 (000b)	CCs are not synchronized
1 (001b)	CCs are synchronized to the pixel clock of the primary camera
2 (010b)	CCs are synchronized to the pixel clock of the secondary camera
3 (011b)	Each set of CCs are synchronized to the pixel clock of their corresponding camera. In other words, the CCs on the primary connector are synchronized to the primary camera's pixel clock, and the CCs on the secondary camera are synchronized to secondary camera's pixel clock.
4 (100b)	Reserved
5 (101b)	Reserved
6 (110b)	Reserved
7 (111b)	Reserved

EN_TRIGGER R/W, CON5[30], Alta, Karbon, Neon, R64

This bitfield has the following properties.

EN_TRIGGER	Meaning
0	External (HW) selected trigger is disabled.
1	External (HW) selected trigger is enabled.

EN_ENCODER R/W, CON5[31], Alta, Karbon, Neon, R64

This bitfield has the following properties.

EN_ENCODER	Meaning
0	External (HW) selected encoder is disabled.
1	External (HW) selected encoder is enabled.

5.9 CON6 Register

Bit	Name
0	VCOUNT
1	VCOUNT
2	VCOUNT
3	VCOUNT
4	VCOUNT
5	VCOUNT
6	VCOUNT
7	VCOUNT
8	VCOUNT
9	VCOUNT
10	VCOUNT
11	VCOUNT
12	VCOUNT
13	VCOUNT
14	VCOUNT
15	VCOUNT
16	VCOUNT
17	LAL
18	ENC_DIV, ENC_DIV_M
19	ENC_DIV, ENC_DIV_M
20	ENC_DIV, ENC_DIV_M
21	ENC_DIV, ENC_DIV_M
22	ENC_DIV, ENC_DIV_M
23	ENC_DIV, ENC_DIV_M
24	ENC_DIV, ENC_DIV_M
25	ENC_DIV, ENC_DIV_M
26	ENC_DIV, ENC_DIV_M
27	ENC_DIV, ENC_DIV_M
28	HCOUNT
29	HCOUNT
30	TRIG_QUALIFIED
31	Reserved

VCOUNT RO, CON6[16..0], Alta, Karbon, Neon, R64

This is the value of the VCOUNT, the VCTAB's address counter.

LAL R/W, CON6[17], Alta, Karbon, Neon, R64

LAL stands for Last Active Line. It controls the mode the VCOUNT is read.

LAL	Meaning
0	VCOUNT register reflects the current value of the VCOUNT.
1	VCOUNT register holds the last active line of the previous frame.

ENC_DIV R/W, CON6[27..18], R64

The encoder pulses will be divided down by the number written in this register. If, for example, ENC_DIV[] = 5, for every five pulses on the selected encoder, the divider will supply one pulse to the board. Programming this register to 0 or 1 will both divide by 1.

ENC_DIV_M R/W, CON6[27..18], Karbon, Neon, R64

This register represents the "M" parameter of the encoder divider equation. See Section 5.1 for more information.

HCOUNT R/W, CON6[29..28], Alta, Karbon, Neon, R64

This register reflects the current value of the two LSBs of the HCOUNT. Reading this register and observing changes in its value means that the HCOUNT is cycling.

TRIG_ QUALIFIED RO, CON6[31], Alta, Karbon, Neon, R64

This is the current state of the selected (via SEL_TRIG) trigger input.

5.10 CON7 Register

Bit	Name
0	AQ_COUNT
1	AQ_COUNT
2	AQ_COUNT
3	AQ_COUNT
4	AQ_COUNT
5	AQ_COUNT
6	AQ_COUNT
7	AQ_COUNT
8	AQ_COUNT
9	AQ_COUNT
10	AQ_COUNT
11	AQ_COUNT
12	AQ_COUNT
13	AQ_COUNT
14	AQ_COUNT
15	AQ_COUNT
16	AQ_COUNT
17	AQ_COUNT
18	AQ_COUNT
19	AQ_COUNT
20	SEL_REG_GEN
21	SEL_REG_GEN
22	GEN_ONESHOT
23	Reserved
24	TAG_BANK
25	TAG_BANK
26	TAG_BANK
27	TAG_BANK
28	TAG_BANK
29	TAG_BANK
30	NTG_TO_ENC
31	NTG_TO_TRIG

AQ_COUNT R/W, CON7[19..0], Alta, Karbon, Neon, R64

The number N written in this register is used to tell the acquisition logic to FREEZE acquisition after N frames have been acquired. The register FREEZE_CON code must be set to 1.

SEL_REG_GEN R/W, CON7[21..20], Alta, Karbon, Neon, R64

Future use.

GEN_ONESHOT R/W, CON7[22], R64

This bit controls the mode of the special signal generator available in the TVI camera specific firmware.

GEN_ONESHOT	Meaning
0	Signal generator is free running.
1	Signal generator synchronized to the external encoder signal.

TAG_BANK RO, CON7[29..24], R64

This is the calculated bank from the address generator latched by the TAG QUAD; diagnostics/test register.

NTG_TO_ENC R/W, CON7[30], Kebon, Neon

This bit provides the ability for the NTG timing generator to rung the encoder input directly. This bit overrides the selection made by the SEL_ENC bit..

NTG_TO_ENC	Meaning
0	The encoder circuit is driven by the selected externel encoder souce.
1	The encoder circuit is driven by the NTG.

NTG_TO_TRIG R/W, CON7[31], Karbon, Neon

This bit provides the ability for the NTG timing generator to rung the trigger input directly. This bit overrides the selection made by the SEL_TRIG bit..

NTG_TO_TRIG	Meaning
0	The trigger circuit is driven by the selected externel trigger souce.
1	The trigger circuit is driven by the NTG.

5.11 CON8 Register

Bit	Name
0	GPOUT0_CON
1	GPOUT0_CON
2	GPOUT0_CON
3	GPOUT1_CON
4	GPOUT1_CON
5	GPOUT1_CON
6	GPOUT2_CON
7	GPOUT2_CON
8	GPOUT2_CON
9	GPOUT3_CON
10	GPOUT3_CON
11	GPOUT3_CON
12	GPOUT4_CON
13	GPOUT4_CON
14	GPOUT4_CON
15	GPOUT5_CON
16	GPOUT5_CON
17	GPOUT5_CON
18	GPOUT6_CON
19	GPOUT6_CON
20	GPOUT6_CON
21	AFPDF
22	AFPDF
23	Reserved
24	RLE_LOAD_H
25	RLE_LOAD_H
26	RLE_LOAD_H
27	RLE_LOAD_H
28	RLE_LOAD_V
29	RLE_LOAD_V
30	RLE_LOAD_V
31	RLE_LOAD_V

GPOUT0_CON R/W, CON8[2..0], Alta, Karbon, Neon, R64

This register selects the signal steered to GPOUT0 on the IO connector

GPOUT0_CON	Selected signal steered to GPOUT0
0 (000b)	GPOUT0 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	The encoder input signal is routed to the GPOUT0 output signal.

GPOUT1_CON R/W, CON8[5..3], Alta, Karbon, Neon, R64

This register selects the signal steered to GPOUT1 on the IO connector

GPOUT1_CON	Selected signal steered to GPOUT1
0 (000b)	GPOUT1 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	The trigger input signal is routed to the GPOUT1 output signal.

GPOUT2_CON R/W, CON8[8..6], Alta, Karbon, Neon, R64

This register selects the signal steered to GPOUT2 on the IO connector

GPOUT2_CON	Selected signal steered to GPOUT2
0 (000b)	GPOUT2 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT3_CON R/W, CON8[11..9], Alta, Karbon, Neon, R64

This register selects the signal steered to GPOUT3 on the IO connector

GPOUT3_CON	Selected signal steered to GPOUT3
0 (000b)	GPOUT3 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT4_CON R/W, CON8[14..12], Alta, Karbon, Neon, R64

This register selects the signal steered to GPOUT4 on the IO connector

GPOUT4_CON	Selected signal steered to GPOUT4
0 (000b)	GPOUT4 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT5_CON R/W, CON8[17..15], Alta, Karbon, Neon, R64

This register selects the signal steered to GPOUT5 on the IO connector

GPOUT5_CON	Selected signal steered to GPOUT5
0 (000b)	GPOUT5 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT6_CON R/W, CON8[20..18], Alta, Karbon, Neon, R64

This register selects the signal steered to GPOUT6 on the IO connector

GPOUT6_CON	Selected signal steered to GPOUT6
0 (000b)	GPOUT6 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

AFPDF R/W, CON8[22..21], Karbon, Neon

This register provides the ability from multiple camera frames to be DMAed as a signle DMA frame. This helps reduce the interrupt rate for very high speed camers.sr

AFPDF	Meaning
0 (00b)	1 camera frame per DMA frame
1 (01b)	16 camera frames per DMA frame
2 (10b)	128 camera frames per DMA frame
3 (11b)	1024 camera frames per DMA frame

RLE_LOAD_H R/W, CON8[27..24], Karbon, Neon

For boards that use RLE CTabs, this register controls the location that the horizontal RLE counter jumps to when the LEN signal is asserted. The units of value in this bit-field is RLE entry, not the CTAB location. In other words, if the jump point is 0x8000 CTAB location, but the RLE entry for this location is 3, then this register should be programmed to 3.

RLE_LOAD_V R/W, CON8[31..28], Karbon, Neon

For boards that use RLE CTabs, this register controls the location that the vertical RLE counter jumps to when the FEN signal is asserted. The units of value in this bitfield is RLE entry, not the CTAB location. In other words, if the jump point is 0x20000 CTAB location, but the RLE entry for this location is 3, then this register should be programmed to 3.

5.12 CON9 Register

Bit	Name
0	MUX_REV
1	MUX_REV
2	MUX_REV
3	MUX_REV
4	MUX_REV
5	MUX_REV
6	MUX_REV
7	MUX_REV
8	MUX_REV
9	MUX_REV
10	MUX_REV
11	MUX_REV
12	TRIM
13	TRIM
14	TRIM
15	TRIM
16	FW_TYPE
17	FW_TYPE
18	FW_TYPE
19	FW_TYPE
20	DISPLAY
21	CLIP
22	SHORT_FRAME
23	RST_CALC_BANK
24	CALC_BANK
25	CALC_BANK
26	CALC_BANK
27	CALC_BANK
28	CALC_BANK
29	CALC_BANK
30	ACPL_MUL
31	ACPL_MUL

MUX_REV RO, CON9[11..0], Alta, Karbon, Neon, R64

Firmware revision.

TRIM R/W, CON9[15..12], Alta, Karbon, Neon, R64

This bit field will delay the LEN relative to the video. The delay, in units of pixels, equals the number programmed in the TRIM[] field.

The net effect for a simple, one tap camera will be a shifting to the left of the displayed image. For multi-tap cameras the visual effect is more complex and depends on the CCD architecture.

The purpose of this bit field is to align the image presented by the different taps. This bit field has the opposite effect of the DELAY field in CON14.

TRIM	Meaning
0 (000b)	LEN is not delayed
1 (001b)	LEN is delayed by 1 clocks
2 (010b)	LEN is delayed by 2 clocks
3 (011b)	LEN is delayed by 3 clocks
4 (100b)	LEN is delayed by 4 clocks
5 (101b)	LEN is delayed by 5 clocks
6 (11ob)	LEN is delayed by 6 clocks
7 (111b)	LEN is delayed by 7 clocks

FW_TYPE RO, CON9[19..16], Alta, Karbon, Neon, R64

Firmware type.

DISPLAY R/W, CON9[20], Alta, Karbon, Neon, R64

This bit controls the acquisition of data that is more than 8 bits/pixel. When this bit is set, only the 8 LSB of the data will be acquired in each lane. To be able to display the 8 MSB (or any other consecutive group of 8 bits), the data must be shifted accordingly with the barrel shifter. For 9 to 16-bit cameras, setting this bit will result in an 8-bit dis-

playable pixel. For high bit depth color cameras, setting this bit will result in a 24-bit color displayable pixel. In both cases. the barrel shifter must be set correctly to get the displayable bits out of the incoming pixels.

DISPLAY	Meaning
0	Acquire full bit depth.
1	Acquire 8 LSBs of each data lane.

CLIP R/W, CON9[21], Alta, Karbon, Neon, R64

This bit will clip the upper and lower 15 gray levels. This is useful for displaying gray level images on VGA monitors set in 256 colors mode. The upper and lower 15 gray levels are dedicated to Windows graphics.

CLIP	Meaning
0	Acquire data as is.
1	Clip upper and lower 15 gray levels to 240 and 15 respectively.

SHORT_FRAME R/W, CON9[22], Alta, Karbon, Neon, R64

Future use.

RST_CALC_ BANK R/W, CON9[23], Alta, Karbon, Neon, R64

For normal operation this bit should be 0.

RST_CALC_BANK	Meaning
0	Normal operation
1	Reset the calculated starting bank.

CALC_BANK RO, CON9[29..24], Alta, Karbon, Neon, R64

Value of the current calculated starting bank.

ACPL_MUL R/W, CON9[31..30], Alta, Karbon, Neon, R64

This register is used to increase the maximum line size the board can acquire. The settings act as multiplier for the ACPL (Active Clocks Per Line) register.

ACPL_MUL	Meaning
0 (00b)	Normal operation. ACPL is used as is
1 (01b)	ACPL is multiplied by 2
2 (10b)	Reserved
3 (11b)	Reserved

5.13 CON10 Register

Bit	Name
0	ACPL
1	ACPL
2	ACPL
3	ACPL
4	ACPL
5	ACPL
6	ACPL
7	ACPL
8	ACPL
9	ACPL
10	ACPL
11	ACPL
12	ACPL
13	ACPL
14	ACPL
15	ACPL
16	ACPL
17	FORMAT
18	FORMAT
19	FORMAT
20	FORMAT
21	FORMAT
22	VID_SOURCE
23	VID_SOURCE
24	VID_SOURCE
25	VID_SOURCE
26	PIX_DEPTH
27	PIX_DEPTH
28	PIX_DEPTH
29	PIX_DEPTH
30	PIX_DEPTH
31	FORCE_8BIT

ACPL R/W, CON10[16..0], Alta, Karbon, Neon, R64

This register defines the Active Clocks Per Line of the horizontal acquisition window. Let's assume for example a single tap camera with 2K pixels per line. If we want to acquire 400 pixels per line, the ACLP will be programmed to 400. For a 2-tap odd-even pixels camera, with 2K pixels per line, to acquire 400 pixels the ACLP will be programmed with the value 200, as for every clock the camera supplies two pixels.

FORMAT RO, CON10[21..17], Alta, Karbon, Neon, R64

This register defines the camera(s) format in terms of taps and scanning architecture. For every FORMAT there is an associated firmware that is downloaded in the FPGAs. The firmware is identified in the camera file by the FORMAT.

FORMAT	Firmware Name	Format Description
0 (00000b)	MUX	1 tap cameras
1 (00001b)	MUX_2TOEP	2 taps, odd-even pixels
2 (00010b)	MUX_2TOEL	2 taps, odd-even lines
3 (00011b)	MUX_2TS	2 taps, segmented
4 (00100b)	MUX_2TS1RI	2 taps, segmented, right inverted
5 (00101b)	MUX_4TS	4 taps, segmented
6 (00110b)	MUX_4T2S2RIOEP	4 taps, odd-even pixels, right taps inverted
7 (00111b)	MUX_4TQ2RI2BU	4 quads, right quads inverted, bottom quads upside down
8 (01000b)	MUX_2CAM	2 cameras: 1 tap each
9 (01001b)	MUX_2CAM_2TOEP	2 cameras: 2 taps, odd-even pixels
10 (01010b)	MUX_2CAM_2TS1RI	2 cameras: 2 taps, segmented, right-inverted
11 (01011b)	MUX_2CAM_2TS	2 cameras: 2 taps, segmented
12 (01100b)	MUX_2CAM_2TOEL	2 cameras: 2 taps, odd-even lines
13 (01101b)	MUX_8TS	8 taps, segmented
14 (01110b)	MUX_BAY	Bayer decoder, 1 tap 8 bit
15 (01111b)	MUX_BAY_OE	Bayer decoder, 2 taps, odd-even pixels
16 (10000b)	MUX_BAY_2TS	Bayer decoder, 2 taps, segmented
17 (10001b)	MUX_4WI	4 taps, 4-way interleaved
18 (10010b)	MUX_2TOEPI	2 taps, odd-even pixels, both inverted
19 (10011b)	MUX_1TI	1 tap, inverted
20 (10100b)	MUX_8WI	8 taps, 8-way interleaved

FORMAT	Firmware Name	Format Description
21 (10101b)	MUX_BAY_2TS_RI	Bayer decoder, 2 taps, segmented, right inverted
22 (10110b)	MUX_4TS2RI	Four taps, segmented, right two taps inverted
23 (10111b)	MUX_8TSOEP4RI	Eight taps, segments, odd/even pixel, for right taps inverted
24 (11000b)	MUX_10WI	Ten taps, interleaved

VID_SOURCE R/W, CON10[25..22], Alta, Karbon, Neon, R64

This register defines the video source and the pattern for the synthetic video. The synthetic patterns appear on all 8 taps, except for code 9.

VID_SOURCE	Video source
0 (0000b)	Camera
1 (0001b)	Camera, special mode for cameras that do not assert the VALID signal.
2 (0010b)	reserved
3 (0011b)	Synthetic horizontal static wedge
4 (0100b)	Synthetic dynamic wedge
5 (0101b)	Synthetic 00h
6 (0110b)	Synthetic FFh
7 (0111b)	Synthetic AAh
8 (1000b)	Synthetic 55h
9 (1001b)	Synthetic ABCDEF0123456789h
10 (1010b)	Synthetic vertical static wedge

PIX_DEPTH R/W, CON10[30..26], Alta, Karbon, Neon, R64

This register defines the pixel depth as well as the color order and packing mode for RGB cameras.

PIX_DEPTH	Bit/pixel, color order and packing
0 (0000b)	8 bits
1 (0001b)	10 bits
2 (0010b)	12 bits
3 (0011b)	14 bits
4 (0100b)	16 bits
5 (0101b)	3x8 bits BGR, DMAed as 32 bits, upper MSB set to 00h
6 (0110b)	3x8 bits BGR, DMAed as 24 bits (packed)
7 (0111b)	3x10 bits RGB, DMAed as 32 bits, display mode is 24 bits
8 (1000b)	3x12 bits RGB, DMAed as 48 bits (packed), display mode is 24 bits
9 (1001b)	32 bits
10 (1010b)	64 bits
11 (1011b)	3x8 bits RGB, DMAed as 32 bits, upper MSB set to 00h
12 (1100b)	3x8 bits RGB, DMAed as 24 bits (packed)
13 (1101b)	3x10 BGR, DMAed as 32 bits, display mode is 24 bits
14 (1110b)	3x12 BGR, DMAed as 48 bits (packed), display mode is 24 bits

FORCE_8BIT R/W, CON10[31], Alta, Karbon, Neon, R64

This bitfield has the following properties.

FORCE_8BIT	Meaning
0 (000b)	Normal operation
1 (001b)	Only 8 LSB of pixel will be acquired

5.14 CON11 Register

Bit	Name
0	ALAST_ADD
1	ALAST_ADD
2	ALAST_ADD
3	ALAST_ADD
4	ALAST_ADD
5	ALAST_ADD
6	ALAST_ADD
7	ALAST_ADD
8	ALAST_ADD
9	ALAST_ADD
10	ALAST_ADD
11	ALAST_ADD
12	ALAST_ADD
13	ALAST_ADD
14	ALAST_ADD
15	DPM_WP
16	BLAST_ADD
17	BLAST_ADD
18	BLAST_ADD
19	BLAST_ADD
20	BLAST_ADD
21	BLAST_ADD
22	BLAST_ADD
23	BLAST_ADD
24	BLAST_ADD
25	BLAST_ADD
26	BLAST_ADD
27	BLAST_ADD
28	BLAST_ADD
29	BLAST_ADD
30	BLAST_ADD
31	UART_MASTER

ALAST_ADD RO, CON11[14..0], Alta, Karbon, Neon, R64

Last address for lane A (used for diagnostics).

DPM_WP R/W, CON11[15], Alta, Karbon, Neon, R64

Prevents the DPM memory from be written by the acquisiton engine. Should normally be set to 0.

BLAST_ADD RO, CON11[30..16], Alta, Karbon, Neon, R64

Last address for lane B (used for diagnostics).

UART_MASTER R/W, CON11[31], Karbon

This bit controls which Karbon VFG is in control of the UART. Poke this bit to one in order to take control of the UART.

5.15 CON12 Register

Bit	Name
0	CLAST_ADD
1	CLAST_ADD
2	CLAST_ADD
3	CLAST_ADD
4	CLAST_ADD
5	CLAST_ADD
6	CLAST_ADD
7	CLAST_ADD
8	CLAST_ADD
9	CLAST_ADD
10	CLAST_ADD
11	CLAST_ADD
12	CLAST_ADD
13	CLAST_ADD
14	CLAST_ADD
15	Reserved
16	DLAST_ADD
17	DLAST_ADD
18	DLAST_ADD
19	DLAST_ADD
20	DLAST_ADD
21	DLAST_ADD
22	DLAST_ADD
23	DLAST_ADD
24	DLAST_ADD
25	DLAST_ADD
26	DLAST_ADD
27	DLAST_ADD
28	DLAST_ADD
29	DLAST_ADD
30	DLAST_ADD
31	RGBHSI

CLAST_ADD RO, CON11[14..0], Alta, Karbon, Neon, R64

Last address for lane C (used for diagnostics).

DLAST_ADD R/W, CON11[30..16], Alta, Karbon, Neon, R64

Last address for lane D (used for diagnostics).

RGBHSI R/W, CON11[31], Alta

Onboards that can do real time color conversion from RGB to HSI color space, the board controls what color space is put out..

RGBHSI	Meaning
0	Output RGB
1	Output HSI

5.16 CON13 Register

Bit	Name
0	VIDEO_MASK
1	VIDEO_MASK
2	VIDEO_MASK
3	VIDEO_MASK
4	VIDEO_MASK
5	VIDEO_MASK
6	VIDEO_MASK
7	VIDEO_MASK
8	VIDEO_MASK
9	VIDEO_MASK
10	VIDEO_MASK
11	VIDEO_MASK
12	VIDEO_MASK
13	VIDEO_MASK
14	VIDEO_MASK
15	VIDEO_MASK
16	VIDEO_MASK
17	VIDEO_MASK
18	VIDEO_MASK
19	VIDEO_MASK
20	VIDEO_MASK
21	VIDEO_MASK
22	VIDEO_MASK
23	VIDEO_MASK
24	VIDEO_MASK
25	VIDEO_MASK
26	VIDEO_MASK
27	VIDEO_MASK
28	VIDEO_MASK
29	VIDEO_MASK
30	VIDEO_MASK
31	VIDEO_MASK

VIDEO_MASK R/W, CON13[31..0], Alta, Karbon, Neon, R64

With the aid of this mask, individual bits in the video data stream can be set to 0. The 32 bit mask is duplicated for the 32 MSB of a 64 bit word.

Bit N in VIDEO_MASK	Meaning
0	Set bit N to 0
1	Pass bit N as is

5.17 CON14 Register

Bit	Name
0	SWRESET
1	FENPOL
2	LENPOL
3	BUTTONS
4	BUTTONS
5	BUTTONS
6	BUTTONS
7	BUTTONS
8	BUTTONS
9	BUTTONS
10	BUTTONS
11	BUTTONS
12	BUTTONS
13	BUTTONS
14	BUTTONS
15	BUTTONS
16	SHIFT_RAW
17	SHIFT_RAW
18	SHIFT_RAW
19	SHIFT_RAW
20	SHIFT_RAW_LEFT
21	DELAY
22	DELAY
23	DELAY
24	SWAP
25	UART_CON
26	UART_CON
27	Reserved
28	DPM_SPLIT
29	DPM_SPLIT
30	DPM_SPLIT
31	DPM_SPLIT

SW_RESET WO, CON14[0], Alta, Karbon, Neon, R64

This bit will always read back 0.

SW_RESET	Meaning
0	Reset de-asserted
1	General reset to acquisition circuitry.

FENPOL R/W, CON14[1], Alta, Karbon, Neon, R64

This bitfield has the following properties.

FENPOL	Meaning
0	FEN is asserted on rising edge.
1	FEN is asserted on falling edge.

LENPOL R/W, CON14[2], Alta, Karbon, Neon, R64

This bitfield has the following properties.

LENPOL	Meaning
0	LEN is asserted on rising edge.
1	LEN is asserted on falling edge.

BUTTONS R/W, CON14[15..3], Alta, Karbon, Neon, R64

R/W register for test/diagnostics.

SHIFT_RAW R/W, CON14[19..16], Alta, Karbon, Neon, R64

This register defines for the barrel shifter the amount of shift for the data to be acquired

SHIFT_RAW_LEFT R/W, CON14[20], Alta, Karbon, Neon, R64

This register defines for the barrel shifter the shift direction for the data to be acquired.

SHIFT_RAW_LEFT	Meaning
0	Shift right
1	Shift left

DELAY R/W, CON14[23..21], Alta, Karbon, Neon, R64

This register is used for aligning the Horizontal Active Window (HAW) relative the Line ENable signal (LEN). If the first active pixel occurs simultaneously with the assertion of LEN, then no delay is needed. If the first active pixel occurs between 1 and 7 clocks later than LEN, the DELAY register must be programmed accordingly. The CTABs can be used to compensate for delays over 7 clocks. However, the granularity of the CTABs is 8 clocks, so both DELAY and the CTABS may have to be used in together to accommodate for some delays.

The net effect for a simple, one tap camera will be a shifting to the right of the displayed image. For multi-tap cameras the visual effect is more complex and depends on the taps architecture. All taps are delayed by the same amount.

The purpose of this bit field is to align the image presented by the different taps. This bit field has the opposite effect of the TRIM field in CON9.

DELAY	Meaning
0 (000b)	HAW is not delayed
1 (001b)	HAW is delayed by 1 clocks
2 (010b)	HAW is delayed by 2 clocks
3 (011b)	HAW is delayed by 3 clocks
4 (100b)	HAW is delayed by 4 clocks
5 (101b)	HAW is delayed by 5 clocks
6 (11ob)	HAW is delayed by 6 clocks
7 (111b)	HAW is delayed by 7 clocks

SWAP R/W, CON14[24], Alta, Karbon, Neon, R64

Future use.

UART_CON R/W, CON14[26..25], Alta, Karbon, Neon, R64

This register will control the connection of the serial ports of the two camera Link connectors.

UART_CON	Connection
0 (00b)	On-board UART connected to CL serial port of main connector
1 (01b)	On-board UART connected to CL serial port of auxiliary connector
2 (10b)	Serial port of main connector CL connected to external serial port, through the IO connector.
3 (11b)	Serial port of auxiliary connector CL connected to external serial port, through the IO connector

DPM_SPLIT R/W, CON14[31..28], Alta, Karbon, Neon, R64

This register controls how incoming data is written to the DPM.

DPM_SPLIT	Mode
0 (0000b)	Normal mode
1 (0001b)	Each tap's output is split in half.
2 (0010b) to 14 (1110b)	Reserved
15 (1111b)	Each tap's output is written in 4K chunks

5.18 CON15 Register

Bit	Name
0	QENC_INTRVL_LL
1	QENC_INTRVL_LL
2	QENC_INTRVL_LL
3	QENC_INTRVL_LL
4	QENC_INTRVL_LL
5	QENC_INTRVL_LL
6	QENC_INTRVL_LL
7	QENC_INTRVL_LL
8	QENC_INTRVL_LL
9	QENC_INTRVL_LL
10	QENC_INTRVL_LL
11	QENC_INTRVL_LL
12	QENC_INTRVL_LL
13	QENC_INTRVL_LL
14	QENC_INTRVL_LL
15	QENC_INTRVL_LL
16	QENC_INTRVL_LL
17	QENC_INTRVL_LL
18	QENC_INTRVL_LL
19	QENC_INTRVL_LL
20	QENC_INTRVL_LL
21	QENC_INTRVL_LL
22	QENC_INTRVL_LL
23	QENC_INTRVL_LL
24	QENC_DECODE
25	QENC_AQ_DIR
26	QENC_AQ_DIR
27	QENC_INTRVL_MODE
28	QENC_NO_REAQ
29	QENC_DUAL_PHASE
30	SCAN_STEP_TRIG
31	QENC_RESET

QENC_INTRVL_LL R/WR/W, CON15[23..0], Karbon, Neon

This register contains the lower limit value that is used to start acquisition when the system is in interval mode (see QENC_INTRVL_MODE).

QENC_DECODE R/W, CON15[24], Karbon, Neon

This bit determines how often the quadrature counter is incremented.

QENC_DECODE	Meaning
0	Counter increments on the rising edge of input A and the rising edge of input B. This is also called "2x" modes.
1	Counter increments on both the rising and falling edge of A and both the rising and falling edge of B. This is also called "4x" mode.

QENC_AQ_DIR R/W, CON15[26..25], Karbon, Neon

This bit controls which quadrature encoder direction is used for acquisition.

QENC_AQ_DIR	Meaning
0 (00b)	Lines are acquired in both directions
1 (01b)	Lines are acquired only in the positive direction.
2 (10b)	Lines are acquired only in the negative direction.
3 (11b)	Reserved

QENC_INTRVL_MODE R/W, CON15[27], Karbon, Neon

When this bit is 1, interval mode is turned on. When interval mode is on, lines are only capture when the encoder counter is between the lower limit (set by QENC_INTRVL_LL) and the upper limit (set by QENT_INTRVL_UL). If the counter is outside of this range, lines are not acquired. Whether lines are acquired as the counter increments through the interval, or decrements through the interval, or in both directions is controlled by QENC_AQ_DIR.

QENC_NO_REAQ R/W, CON15[28], Karbon, Neon

This bit controls how the quadrature encoder system handles the situation where the encoder does not smoothly increase (or decrease if QENC_AQ_DIR = 1). If there is "jitter" in the encoder signal, often caused by problems with the mechanical systems, it is possible for the board to acquire the same line or lines more than once as the

mechanical system backs up and moves forward (jitter). This re-acquisition can cause problems as the resulting images will have distortions and will not accurately represent the object in front of the camera.

Programming this bit to a 1 turns on the no-reacquisition circuit. This circuit eliminates this problem as each line in the image will only be acquired once, regardless of how much jitter occurs in the quadrature encoder input. The circuit does this by making sure that only one line is acquired for each encoder counter value. If the quadrature encoder backs up, and then moves forward, the board will not acquire lines until a new encoder counter value is reached.

This system handles any amount of jitter, regardless of how many times the counter passes through a value, or to what extremes the counter goes. New lines will only be acquired when new values are reached.

Once the entire frame has been acquired, the system must be reset. The system can always be reset by poking QENC_RESET to 1. There are also ways that the system can automatically be reset, see QENC_RESET_MODE.

QENC_NO_REAQ	Meaning
0	Lines are acquired every change in the encoder counter (as controlled by QENC_AQ_DIR)
1	Lines are only acquired when the encoder counter reaches new values (also controlled by QENC_AQ_DIR)

QENC_DUAL_PHASE R/W, CON15[29], Karbon, Neon

This bit controls which type of encoder is attached.

QENC_DUAL_PHASE	Meaning
0	A single phase encoder is attached
1	A quadrature encoder is attached

SCAN_STEP_TRIG R/W, CON15[30], Karbon, Neon

The scan step circuit uses the encoder to generate a trigger to the system. The scan step trigger generates a trigger every N lines (N is set in the SCAN_STEP register).

SCAN_STEP_TRIG	Meaning
0	Trigger comes of the normal source
1	Trigger comes from the scan step circuit

QENC_RESET WO, CON15[31], Karbon, Neon

Poking this bit to a 1 resets the entire quadrate encoder system.

5.19 CON16 Register

Bit	Name
0	QENC_INTRVL_UL
1	QENC_INTRVL_UL
2	QENC_INTRVL_UL
3	QENC_INTRVL_UL
4	QENC_INTRVL_UL
5	QENC_INTRVL_UL
6	QENC_INTRVL_UL
7	QENC_INTRVL_UL
8	QENC_INTRVL_UL
9	QENC_INTRVL_UL
10	QENC_INTRVL_UL
11	QENC_INTRVL_UL
12	QENC_INTRVL_UL
13	QENC_INTRVL_UL
14	QENC_INTRVL_UL
15	QENC_INTRVL_UL
16	QENC_INTRVL_UL
17	QENC_INTRVL_UL
18	QENC_INTRVL_UL
19	QENC_INTRVL_UL
20	QENC_INTRVL_UL
21	QENC_INTRVL_UL
22	QENC_INTRVL_UL
23	QENC_INTRVL_UL
24	QENC_REAQ_MODE
25	QENC_REAQ_MODE
26	QENC_RESET_REAQ
27	ENC_DIV_FORCE_DC
28	ENC_DIV_OPEN_LOOP
29	ENC_DIV_FCLK_SEL
30	ENC_DIV_FCLK_SEL
31	ENC_DIV_FCLK_SEL

QENC_INTRVL_UL R/W, CON16[23..0], Karbon, Neon

This register contains the upper limit value that is used to start acquisition when the system is in interval mode (see QENC_INTRVL_MODE).

QENC_REAQ_MODE R/W, CON16[25..24], Karbon, Neon

This bit controls how the circuit that prevents re-acquisition from encoder jitter is reset. Re-acquisition is prevented by keeping a list of lines that have been acquired, and making sure the only lines that are not on the list are acquired. Once the entire frame is acquired, there must be some way to reset the list, otherwise no new lines will be acquired during the next frame. See QENC_NO_REAQ for more information.

QENC_REAQ_MODE	Meaning
0 (00b)	Reset the list of acquired lines when QENC_RESET_REAQ is poked to 1.
1 (01b)	Reset the list of lines when the encoder counter is outside of the interval set by the upper limit and lower limit. Whether the reset occurs above the upper limit or below the lower limit depens on the QENC_AQ_DIR register.
2 (10b)	Reserved
3 (11b)	Reserved

QENC_RESET_REAQ WO, CON16[26], Karbon, Neon

This register is used to reset the circuit that prevents the re-acquisition of lines when QENC_NO_REAQ is set to 1. Writing a 1 to this register deletes the list of acquired lines, thus next time the lines are passed over, they will be acquired again. Writing to this bit always resets the no re-acquistiion circuit, regardless of the mode as set by the QENC_REAQ_MODE. However, the register QENC_REAQ_MODE can be used to put the board in a mode where the no re-aquisition circuit is reset automatically every pass over the image.

ENC_DIV_FORCE_DC R/W, CON16[27], R64, Karbon, Neon

This register is used to controls the behavior of the encoder divider when input frequency falls below the minimum.

ENC_DIV_FORCE_DC	Meaning
0	Encoder divider runs in simple divider mode.
1	Encoder divider output stops (goes to DC).

ENC_DIV_ OPEN_LOOP

R/W, CON16[28], R64, Karbon, Neon

This register controls whether the output signal phase of the Encoder Divider is lock to the intput or is allowed to free run.

ENC_DIV_OPEN_LOOP	Meaning
0	Output phased locked to input
1	Ouput runs open loop

ENC_DIV_FCLK_ SEL

R/W, CON16[31..29], R64, Karbon, Neon

This register is reserved for future support for alternate Encoder Divider PLL Master clock frequencies. Currently must be set to 0, which selects 50 MHz clock

5.20 CON17 Register

Bit	Name
0	NTG_RATE
1	NTG_RATE
2	NTG_RATE
3	NTG_RATE
4	NTG_RATE
5	NTG_RATE
6	NTG_RATE
7	NTG_RATE
8	NTG_RATE
9	NTG_RATE
10	NTG_RATE
11	NTG_RATE
12	NTG_RATE
13	NTG_RATE
14	NTG_RATE
15	NTG_RATE
16	NTG_RATE
17	NTG_RATE
18	NTG_RATE
19	NTG_RATE
20	NTG_RATE
21	NTG_RATE
22	NTG_RATE
23	NTG_RATE
24	NTG_RATE
25	NTG_RATE
26	NTG_RATE
27	NTG_RATE
28	Reserved
29	Reserved
30	NTG_ONESHOT
31	NTG_TRIG_MODE

NTG_RATE R/W, CON17[27..0], Alta, Karbon, Neon, R64

This register controls the line/frame rate period of the NTG. One LSB in this registers represents on clock period of the NTG clock. The NTG clock frequency depends on the model Table 5-3. See Section 3.1 for more information.

Table 5-3 NTG clock frequency

Model	Frequency
Karbon, Neon, R64	7.3728 MHz
Alta	5.000 MHz

NTG_ONESHOT R/W, CON17[30], Alta, Karbon, Neon, R64

This bit defines whether the NTG is free running or in one shot mode.

NTG_ONESHOT	Mode
0	NTG is free running
1	NTG is in one shot mode

NTG_TRIG_ MODE R/W, CON17[31], Alta, Karbon, Neon, R64

This bit determines what triggers the NTG when it is in one shot mode.

NTG_ONESHOT	Mode
0	NTG is triggered by the selected trigger signal
1	NTG is triggered by the selected encoder signal

5.21 CON18 Register

Bit	Name
0	ALPF
1	ALPF
2	ALPF
3	ALPF
4	ALPF
5	ALPF
6	ALPF
7	ALPF
8	ALPF
9	ALPF
10	ALPF
11	ALPF
12	ALPF
13	ALPF
14	ALPF
15	ALPF
16	ALPF
17	TOP_REV
18	TOP_REV
19	TOP_REV
20	TOP_REV
21	TOP_REV
22	TOP_REV
23	TOP_REV
24	TOP_REV
25	TOP_REV
26	TOP_REV
27	TOP_REV
28	TOP_REV
29	TOP_REV
30	NTG_INVERT
31	NTG_TIME_MODE

ALPF R/W, CON18[16..0], Alta, Karbon, Neon, R64

This register defines the Active Lines Per Frame of the vertical acquisition window. Let's assume for example a single tap camera with 2K lines per frame. If we want to acquire 400 lines per frame, the ALPF will be programmed to 400. For a 2-tap odd-even lines camera, with 2K lines per frame, to acquire 400 pixels the ALPF will be programmed with the value 200, as for every LEN the camera supplies two lines.

TOP_REV RO, CON9[11..0], Alta, Karbon, Neon, R64

Firmware revision.

NTG_INVERT R/W, CON18[30], Alta, Karbon, Neon, R64

This bit allows for the inversion of the New Timing Generators's (NTG) output. See Section 3.1 for more information on the NTG.

NTG_INVERT	Meaning
0	NTG output is asserted high
1	NTG output is asserted low

NTG_TIME_MODE R/W, CON18[31], Alta, Karbon, Neon, R64

This bit is used to scale down the frequency of the NTG clock. The NTG clock frequency depends on the board family. See Section 3.1 for more information. This mode is useful for area scan cameras that need very long exposure times.

NTG_TIME_MODE	Meaning
0	NTG clock is used as is.
1	NTG clock is divided by 128.

5.22 CON19 Register

Bit	Name
0	LINES_TOGO
1	LINES_TOGO
2	LINES_TOGO
3	LINES_TOGO
4	LINES_TOGO
5	LINES_TOGO
6	LINES_TOGO
7	LINES_TOGO
8	LINES_TOGO
9	LINES_TOGO
10	LINES_TOGO
11	LINES_TOGO
12	LINES_TOGO
13	LINES_TOGO
14	LINES_TOGO
15	LINES_TOGO
16	LINES_TOGO
17	ENC_DIV_N
18	ENC_DIV_N
19	ENC_DIV_N
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

LINES_TOGO R/W, CON19[16..0], Alta, Karbon, Neon, R64

This register will reflect the number of remaining lines left to be acquired till the end of the frame.

ENC_DIV_N R/W, CON19[19..17], R64, Karbon, Neon

This register represents the “N” parameter in the encoder divider equation. See Section 5.1 for more information.

5.23 CON20 Register

Bit	Name
0	FIFO_EQ
1	FIFO_EQ
2	FIFO_EQ
3	FIFO_EQ
4	FIFO_EQ
5	FIFO_EQ
6	FIFO_EQ
7	FIFO_EQ
8	VID_BRL
9	VID_BRL
10	VID_BRL
11	VID_BRL
12	VID_BRL
13	VID_BRL
14	VID_BRL
15	VID_BRL
16	VIDEO_2DPM
17	VIDEO_2DPM
18	VIDEO_2DPM
19	VIDEO_2DPM
20	VIDEO_2DPM
21	VIDEO_2DPM
22	VIDEO_2DPM
23	VIDEO_2DPM
24	COLOR_MASK
25	COLOR_MASK
26	SHIFT_DSP_SELECT
27	SHIFT_DSP
28	SHIFT_DSP
29	SHIFT_DSP
30	SHIFT_DSP
31	SHIFT_DSP_LEFT

FIFO_EQS RO, CON20[7..0], Alta, Karbon, Neon, R64

This register reflects the instantaneous value of the 8 LSB of the first tap of the main CL connector. Used for diagnostics/test.

VID_BRL RO, CON20[15..8], Alta, Karbon, Neon, R64

This register reflects the instantaneous value of the 8 LSB of the barrel shifter of lane A. Used for diagnostics/test.

VIDEO_2DPM RO, CON20[23..16], Alta, Karbon, Neon, R64

This register reflects the instantaneous value of the 8 LSB of the video written in the DPM's lane A. Used for diagnostics/test.

COLOR_MASK R/W, CON20[25..24], Alta, Karbon, Neon, R64

This bitfield can be used to mask out color channels when acquiring color pixels formats (e.g 24-bit color, 36-bit color, etc.).

COLOR_MASK	Meaning
0 (00b)	Pass all colors
1 (01b)	Pass only the red channel, set the blue and green channels to 0
2 (10b)	Pass only the green channel, set the blue and red channels to 0
3 (11b)	Pass only the blue channel, set the red and green channels to 0

SHIFT_DSP_SELECT R/W, CON20[26], Alta, Karbon, Neon, R64

This bitfield has the following properties.

SHIFT_DSP_SELECT	Meaning
0	Supply barrel shifter with the acquisition shift code
1	Supply barrel shifter with the display shift code.

SHIFT_DISP R/W, CON20[30..27], Alta, Karbon, Neon, R64

This register holds the shift amount for data to be displayed.

SHIFT_DSP_LEFT R/W, CON20[31], Alta, Karbon, Neon, R64

This bitfield has the following properties.

SHIFT_DSP_LEFT	Meaning
0	Shift display data right
1	Shift display data left.

5.24 CON21 Register (Bayer Version)

Bit	Name
0	RED_GAIN
1	RED_GAIN
2	RED_GAIN
3	RED_GAIN
4	RED_GAIN
5	RED_GAIN
6	RED_GAIN
7	RED_GAIN
8	GREEN_GAIN
9	GREEN_GAIN
10	GREEN_GAIN
11	GREEN_GAIN
12	GREEN_GAIN
13	GREEN_GAIN
14	GREEN_GAIN
15	GREEN_GAIN
16	BLUE_GAIN
17	BLUE_GAIN
18	BLUE_GAIN
19	BLUE_GAIN
20	BLUE_GAIN
21	BLUE_GAIN
22	BLUE_GAIN
23	BLUE_GAIN
24	DECODER_OUT
25	DECODER_OUT
26	DECODER_OUT
27	Reserved
28	BAYER_BIT_DEPTH
29	BAYER_BIT_DEPTH
30	DECODER_PHASE
31	DECODER_PHASE

CON21 is a “soft” register. Soft registers change definitions depending on the version board and the firmware that is downloaded to the board.

REG_GAIN R/W, CON21[7..0], Karbon, R64

This register controls the gain of the red channel. The video value is multiplied by the value in RED_GAIN and after that scaled down by 64. Numbers above 255 are clipped to 255 (saturation effect).

GREEN_GAIN R/W, CON21[15..8], Karbon, R64

This register controls the gain of the green channel. The video value is multiplied by the value in GREEN_GAIN and after that scaled down by 64. Numbers above 255 are clipped to 255 (saturation effect).

BLUE_GAIN R/W, CON21[23..16], Karbon, R64

This register controls the gain of the blue channel. The video value is multiplied by the value in BLUE_GAIN and after that scaled down by 64. Numbers above 255 are clipped to 255 (saturation effect).

DECODER_OUT R/W, CON21[26..24], Karbon, R64

These bits controls the output of the Bayer decoder.

DECODER_OUT	Meaning
0 (000b)	Decode RGB on all three channels
1 (001b)	Raw data on all three channels
2 (010b)	Decode intensity on all three channels
3 (011b)	Decode red on all three channels
4 (100b)	Decode green on all three channels
5 (101b)	Decode blue on all three channels
6 (110b)	Reserved
7 (111b)	Reserved

BAYER_BIT_DEPTH

R/W, CON21[29..28], Karbon, R64

This bit is set if the pixel depth from the camera is 10 bits.

BAYER_10_BIT	Meaning
0 (00b)	8-bit pixels
1 (01b)	12-bit pixels
2 (10b)	10-bit pixels
3 (11b)	Reserved

DECODER_PHASE

R/W, CON21[31..30], Karbon, R64

These bits control the starting phase of the Bayer decoder. This register is set based on the arrangement of the color matrix in the camera's CCD.

DECODER_PHASE	Meaning
0 (00b)	First two pixels: Blue, Green
1 (01b)	First two pixels: Green, Blue
2 (10b)	First two pixels: Red, Green
3 (11b)	First two pixels: Green, Red

5.25 CON22 Register

Bit	Name
0	FLASH_DATA
1	FLASH_DATA
2	FLASH_DATA
3	FLASH_DATA
4	FLASH_DATA
5	FLASH_DATA
6	FLASH_DATA
7	FLASH_DATA
8	FLASH_DATA
9	FLASH_DATA
10	FLASH_DATA
11	FLASH_DATA
12	FLASH_DATA
13	FLASH_DATA
14	FLASH_DATA
15	FLASH_DATA
16	SCAN_STEP
17	SCAN_STEP
18	SCAN_STEP
19	SCAN_STEP
20	SCAN_STEP
21	SCAN_STEP
22	SCAN_STEP
23	SCAN_STEP
24	SCAN_STEP
25	SCAN_STEP
26	SCAN_STEP
27	SCAN_STEP
28	SCAN_STEP
29	SCAN_STEP
30	SCAN_STEP
31	SCAN_STEP

FLASH_DATA R/W, CON22[15..0], Karbon

This bitfield is used for writing to the flash memory on the board.

SCAN_STEP R/W, CON22[31..16], Karbon, Neon

This bitfield controls the number of encoder pulses that must occur before a trigger is issued to the system. See SCAN_STEP_TRIG for more information. The Scan Step circuit takes into account the interval and re-acquisition functions.

5.26 CON23 Register

Bit	Name
0	DPM_SIZE
1	DPM_SIZE
2	DPM_SIZE
3	DPM_SIZE
4	DPM_SIZE
5	DPM_SIZE
6	DPM_SIZE
7	DPM_SIZE
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	CTAB_INT_CON
16	LINES_PER_INT
17	LINES_PER_INT
18	LINES_PER_INT
19	LINES_PER_INT
20	LINES_PER_INT
21	LINES_PER_INT
22	LINES_PER_INT
23	LINES_PER_INT
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

DPM_SIZE RO, CON23[7..0], Alta, Karbon, Neon, R64

This register specifies the size of the DPM in units of 4096 bytes.

CTAB_INT_CON RW, CON23[15], Karbon, Neon, Alta

This bit controls the source of the CTAB interrupt.

CTAB_INT_CON	Meaning
0	CTAB interrupt sourced from CTAB
1	CTAB interrupt sourced from lines per interrupt circuit.

LINES_PER_INT RW, CON23[23..16], Karbon, Neon, Alta

This bit controls the lines per interrupt circuit. This circuit can be used to create a periodic interrupt on the CTAB interrupt. The interrupt rate will be every N lines, where N is the value programmed in this register. Note that CTAB_INT_CON must be set to one in order for the interrupts to be seen by the host.

5.27 CON24 Register

Bit	Name
0	LUT_HOST_DATA
1	LUT_HOST_DATA
2	LUT_HOST_DATA
3	LUT_HOST_DATA
4	LUT_HOST_DATA
5	LUT_HOST_DATA
6	LUT_HOST_DATA
7	LUT_HOST_DATA
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	LUT_ON
16	LUT_HOST_ADDR
17	LUT_HOST_ADDR
18	LUT_HOST_ADDR
19	LUT_HOST_ADDR
20	LUT_HOST_ADDR
21	LUT_HOST_ADDR
22	LUT_HOST_ADDR
23	LUT_HOST_ADDR
24	LUT_BANK
25	LUT_BANK
26	Reserved
27	LUT_DATA_WRITE_SEL
28	LUT_HOST_LANE
29	LUT_HOST_LANE
30	LUT_WEN
31	LUT_HOST_ACCESS

CON24 is a “soft” register. Soft registers change definitions depending on the version board and the firmware that is downloaded to the board.

LUT_HOST_DATA R/W, CON24[7..0], Alta, Karbon, Neon, R64

This register is used to read and write data from the LUT. The LUT is programmed indirectly using this and the other registers in CON24.

The procedure to write data to the LUT is as follows:

Set LUT_HOST_ACCESS to 1.
Set LUT_DATA_WRITE_SEL to 1.
Set LUT_BANK to the desired bank to program.
Set LUT_HOST_LANE to the desired LUT lane to program.
Set LUT_HOST_ADDR to the desired LUT location to program (LUT input).
Set LUT_HOST_DATA to the value desired (LUT output).
Write LUT_WEN to 1, this copies the value from the LUT_HOST_DATA register to the LUT's memory location as specified by LUT_HOST_ADDR.

The procedure to read data from the LUT is as follows:

Set LUT_HOST_ACCESS to 1.
Set LUT_DATA_WRITE_SEL to 0.
Set LUT_BANK to the desired bank to read.
Set LUT_HOST_LANE to the desired LUT lane to read.
Set LUT_HOST_ADDR to the desired LUT location to read.
Read LUT_HOST_DATA, the value returned in this register is the value in the LUT's memory.

LUT_ON R/W, CON24[15], Alta, Karbon, Neon, R64

This register is used to insert or bypass the LUT from the path of incoming camera data.

LUT_ON	Meaning
0	LUT is not in the data path (bypassed)
1	LUT is in the data path

LUT_HOST_ADDR R/W CON24[23..16], Alta, Karbon, Neon, R64

This register is used to set the address for a read operation from the LUT memory or a write operation to the LUT memory. See the description of LUT_HOST_DATA for more details.

LUT_BANK R/W, CON24[25..24], Alta, Karbon, Neon, R64

These bits control which bank of the LUT is being programmed, and which bank is being used to pass image data.

LUT_BANK	Meaning
0 (000b)	Host access to bank 0, data passes through bank 0
1 (001b)	Host access to bank 1, data passes through bank 1
2 (010b)	Host access to bank 2, data passes through bank 2
3 (011b)	Host access to bank 3, data passes through bank 3

LUT_DATA_WRITE_SEL R/W, CON24[27], Alta, Karbon, Neon, R64

This bit is used to control how the LUT data is being accessed.

LUT_DATA_WRITE_SEL	Meaning
0	When reading LUT_HOST_DATA, the register returns the value currently in the LUT. In this mode LUT_HOST_DATA is read only.
1	LUT_HOST_DATA acts like a normal register. It can be written and read normally. The value in the LUT_HOST_DATA register is not transferred to the LUT memory until a 1 is written to LUT_WEN.

LUT_HOST_LANE R/W, CON24[29..28], Alta, Karbon, Neon, R64

These bits control which LUT lane can be access by the host.

LUT_HOST_LANE	Meaning
0 (000b)	Host access to lane 0
1 (001b)	Host access to lane 1
2 (010b)	Host access to lane 2
3 (011b)	Host access to lane 3

LUT_WEN WO, CON24[30], Alta, Karbon, Neon, R64

When LUT_DATA_WRITE_SEL is set to 1, Writing a 1 to this bit causes the value in LUT_HOST_DATA to be transferred to the LUT memory. When LUT_DATA_WRITE_SEL is set to 0, writing to this bit has no effect. See LUT_HOST_DATA for more information.

LUT_HOST_ACCESS

R/W, CON24[31], Alta, Karbon, Neon, R64

These bits turns on and off host access to the LUT..

DECODER_OUT	Meaning
0	The LUT cannot be accessed by the host
1	The LUT can be accessed by the host

5.28 CON25 Register

Bit	Name
0	DELAY_TAP1
1	DELAY_TAP1
2	DELAY_TAP1
3	DELAY_TAP1_SEL
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

DELAY_TAP1 R/W, CON25[2..0], Alta, Karbon, Neon, R64

These bits control the delay for tap 1 only when DELAY_TAP1_SEL = 1. In this mode, tap 0 and tap 1 can be delayed independently. These bits have no effect if DELAY_TAP1_SEL = 0. This register works in a similar manner to the DELAY register.

DELAY_TAP1	Meaning
0 (000b)	HAW is not delayed
1 (001b)	HAW is delayed by 1 clocks
2 (010b)	HAW is delayed by 2 clocks
3 (011b)	HAW is delayed by 3 clocks
4 (100b)	HAW is delayed by 4 clocks
5 (101b)	HAW is delayed by 5 clocks
6 (11ob)	HAW is delayed by 6 clocks
7 (111b)	HAW is delayed by 7 clocks

DELAY_TAP1_SEL R/W, CON25[3], Alta, Karbon, Neon, R64

This bit selects the register that controls the delay for tap 1. Tap 0 is always controlled by the register DELAY.

DELAY_TAP1_SEL	Meaning
0	Tap 1 is controlled by DELAY
1	Tap 1 is controlled by DELAY_TAP1

5.29 CON26 Register

Bit	Name
0	NTG_EXPOSURE
1	NTG_EXPOSURE
2	NTG_EXPOSURE
3	NTG_EXPOSURE
4	NTG_EXPOSURE
5	NTG_EXPOSURE
6	NTG_EXPOSURE
7	NTG_EXPOSURE
8	NTG_EXPOSURE
9	NTG_EXPOSURE
10	NTG_EXPOSURE
11	NTG_EXPOSURE
12	NTG_EXPOSURE
13	NTG_EXPOSURE
14	NTG_EXPOSURE
15	NTG_EXPOSURE
16	NTG_EXPOSURE
17	NTG_EXPOSURE
18	NTG_EXPOSURE
19	NTG_EXPOSURE
20	NTG_EXPOSURE
21	NTG_EXPOSURE
22	NTG_EXPOSURE
23	NTG_EXPOSURE
24	NTG_EXPOSURE
25	NTG_EXPOSURE
26	NTG_EXPOSURE
27	NTG_EXPOSURE
28	Reserved
29	Reserved
30	NTG_RESET
31	NTG_SLAVE

NTG_EXPOSURE R/W, CON26[27..0], Alta, Karbon, Neon, R64

This register controls the exposure period of the NTG. One LSB in this registers represents on clock period of the NTG clock. The NTG clock frequency depends on the model Table 5-4. See Section 3.1 for more information.

Table 5-4 NTG clock frequency

Model	Frequency
Karbon, Neon, R64	7.3728 MHz
Alta	5.000 MHz

NTG_RESET WO, CON26[30], Alta, Karbon, Neon, R64

This bit resets the NTG's internal counter. Writing a 1 to this bit resets the counter to 0.

NTG_SLAVE R/W, CON26[31], Alta, Karbon, Neon, R64

This bit determines how whether the NTG is running on its own timing, or slave to the master VFG.

Note: This bit must be set to 0 for the master VFG.

NTG_SLAVE	Mode
0	NTG is running on its own timing
1	NTG is slaved to the master VFG

5.30 CON27 Register

Bit	Name
0	FLASH_ADDR
1	FLASH_ADDR
2	FLASH_ADDR
3	FLASH_ADDR
4	FLASH_ADDR
5	FLASH_ADDR
6	FLASH_ADDR
7	FLASH_ADDR
8	FLASH_ADDR
9	FLASH_ADDR
10	FLASH_ADDR
11	FLASH_ADDR
12	FLASH_ADDR
13	FLASH_ADDR
14	FLASH_ADDR
15	FLASH_ADDR
16	FLASH_ADDR
17	FLASH_ADDR
18	FLASH_ADDR
19	FLASH_ADDR
20	FLASH_ADDR
21	FLASH_ADDR
22	FLASH_ADDR
23	FLASH_ADDR
24	FLASH_ADDR
25	FLASH_ADDR
26	FLASH_WP
27	FLASH_RST
28	FALSH_BE
29	FLASH_CE
30	FLASH_OE
31	FLASH_WE

FLASH_ADDR R/W, CON27[25..0], Karbon

This register is used for read/writting to the on board flash memoyr.

FLASH_WP R/W, CON27[26], Karbon

This register is used for read/writting to the on board flash memoyr.

FLASH_RST R/W, CON27[27], Karbon

This register is used for read/writting to the on board flash memoyr.

FLASH_BE R/W, CON27[28], Karbon

This register is used for read/writting to the on board flash memoyr.

FLASH_CE R/W, CON27[29], Karbon

This register is used for read/writting to the on board flash memoyr.

FLASH_OE R/W, CON27[30], Karbon

This register is used for read/writting to the on board flash memoyr.

FLASH_WE R/W, CON27[31], Karbon

This register is used for read/writting to the on board flash memoyr.

5.31 CON36 Register

Bit	Name
0	MEM_ADDR_LO
1	MEM_ADDR_LO
2	MEM_ADDR_LO
3	MEM_ADDR_LO
4	MEM_ADDR_LO
5	MEM_ADDR_LO
6	MEM_ADDR_LO
7	MEM_ADDR_LO
8	MEM_ADDR_LO
9	MEM_ADDR_LO
10	MEM_ADDR_LO
11	MEM_ADDR_LO
12	MEM_ADDR_LO
13	MEM_ADDR_LO
14	MEM_ADDR_LO
15	MEM_ADDR_LO
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

MEM_ADDR_LO R/W, CON25[15..0], Neon

This register is the lower 16 bits used to access the flash or ROM memory on boards that have it. This is not a user programmable register.

5.32 CON37 Register

Bit	Name
0	MEM_ADDR_HI
1	MEM_ADDR_HI
2	MEM_ADDR_HI
3	MEM_ADDR_HI
4	MEM_CS
5	MEM_WRITE
6	DWNLD_MODE
7	DWNLD_MODE
8	MEM_DATA
9	MEM_DATA
10	MEM_DATA
11	MEM_DATA
12	MEM_DATA
13	MEM_DATA
14	MEM_DATA
15	MEM_DATA
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

MEM_ADDR_HI R/W, CON37[3..0], Neon

This register is the upper 4 bits used to access the flash or ROM memory on boards that have it. This is not a user programmable register.

MEM_CS R/W, CON37[4], Neon

This bit is the chip select which controls both reading and writing to either the flash or the ROM. This bit controls both host access and FPGA download source.This is not a user programmable register.

MEM_CS	Meaning
0	Host and FPGA access is to/from the ROM
1	Host and FPGA access is to/from the flash

MEM_WRITE R/W, CON37[5], Alta, Neon

Used to write to SRAM. Writing a 1 to this bit force the data in MEM_DATA to be written to the address in MEM_ADDR.

DWNLD_MODE R/W, CON37[7..6], Alta, Neon

Future use.

MEM_DATA R/W, CON37[15..8], Neon

This bitfield provides data access used when reading or writing the flash or ROM on boards that support these features. This is not a user programmable register.

5.33 CON38 Register

Bit	Name
0	POCL_POWER_ON
1	POCL_EN_GND
2	POCL_CLOCK_WAIT
3	Reserved
4	POCL_SENSE
5	POCL_CLK_ DETECTED
6	POCL_DETECTED
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

POCL_POWER_ON RO, CON38[0], Neon

This register indicates the state of the power on the Camera Link connector.

POCL_EN_POWER	Meaning
0	Power is not applied to the power wires on the CL cable.
1	Power is applied to the power wires on the CL cable.

POCL_GND_ON RO, CON38[1], Neon

This register indicates the state of the ground on the Camera Link connector.

POCL_GND_ON	Meaning
0	The power wires on the CL cable are not grounded.
1	The power wires on the CL cable are grounded.

POCL_CLOCK_WAIT RO, CON38[2], Neon

This register indicates that the PoCL state machine is the "waiting for clock" state. In this state, the power has been applied to the camera, but the camera may be powered up yet and may not be output a pixel clock. The PoCL state machine stays in the state for a few seconds, Once it leaves this state, the PoCL state machine will immediately remove the power if it sense that the pixel clock has stopped.

POCL_CLOCK_WAIT	Meaning
0	The PoCL state machine is not in the waiting for clock state.
1	The PoCL state machine is waiting for the pixel from the camera.

POCL_SENSE RO, CON38[3], Neon

This register indicates that the PoCL state machine is the "sense" state. In this state, the powers has not been applied, and the PoCL state machine is watching the impedance on the CL cable. If the impedance of a PoCL camera is detected, the power will be applied. It a short is detected, indicating a legacy camera/cable has been con-

nected, the PoCL power lines will be grounded. The PoCL state machine can stay in this state indefinitely if neither of the above two conditions are detected (i.e. nothing is connected).

POCL_SENSE	Meaning
0	The PoCL state machine is not in the sense state.
1	The PoCL state machine is in the sense state.

POCL_CLK_ DETECTED

RO, CON38[5], Neon

This register indicates that the PoCL state machine is the "PoCL camera clock has been detected" state. This state is the normal powered up steady state for the PoCL state machine.

POCL_CLK_DETECTED	Meaning
0	The PoCL state machine has not detected a camera pixel clock.
1	The PoCL state machine has detected a camera pixel clock.

POCL_ DETECTED

RO, CON38[6], Neon

This register indicates that the PoCL state machine has detected a PoCL camera..

POCL_DETECTED	Meaning
0	The PoCL state machine has not detected a PoCL-camera.
1	The PoCL state machine has detected a PoCL camera.

5.34 CON40 Register

Bit	Name
0	AFE_PORT_ADDR
1	AFE_PORT_ADDR
2	AFE_PORT_ADDR
3	AFE_PORT_ADDR
4	AFE_PORT_ADDR
5	AFE_PORT_ADDR
6	AFE_PORT_ADDR
7	AFE_PORT_ADDR
8	AFE_PORT_WRITE
9	AFE_PORT_ACCESS
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

AFE_PORT_ADDR

R/W, CON40[7..0], Alta

Used to access the AFE. The value written in the register will be used as the address for subsequent read/write operations.

AFE_PORT_WRITE

R/W, CON40[8], Alta

Determines the AFE access operation.

AFE_PORT_WRITE	Meaning
0	The next access operation will be a read.
1	The next access operation will be a write.

AFE_PORT_ACCESS

WO, CON40[9], Alta

Writing a 1 to the bit causes the AFE to be accessed. The type of operation depends on the AFE_PORT_WRITE bit.

5.35 CON41 Register

Bit	Name
0	AFE_PORT_DATA
1	AFE_PORT_DATA
2	AFE_PORT_DATA
3	AFE_PORT_DATA
4	AFE_PORT_DATA
5	AFE_PORT_DATA
6	AFE_PORT_DATA
7	AFE_PORT_DATA
8	AFE_PORT_BUSY
9	AFE_PORT_ERROR
10	AFE_PORT_RESET
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

AFE_PORT_DATA

R/W, CON41[7..0], Alta

Used to access the AFE. The value written in this bitfield will be use written to the AFE during the next write operation. For read operations, the value read from the AFE will be available in this bitfield after the read operation is complete.

AFE_PORT_BUSY

RO, CON41[8], Alta

Used when accessing the AFE.

AFE_PORT_BUSY	Meaning
0	The AFE access operation is completed.
1	The AFE access operation is still taking place, the data address/data ports can not be read/written.

AFE_PORT_ERROR

RO, CON41[9], Alta

A 1 in this bit indicates that an error occurred during the last AFE access operation.

AFE_PORT_RESET

WO, CON41[10], Alta

Writing a 1 to the bit resets the AFE access mechanism.

5.36 CON42 Register

Bit	Name
0	FI
1	FIRST_FI
2	RD_WEN
3	Reserved
4	RD_HD
5	RD_VD
6	SWAP_LINES
7	FI_POL
8	SOE
9	SOE
10	ACQ_IV
11	FEN_SEL
12	FEN_SEL
13	FEN_SEL
14	HD_SEL
15	HD_SEL
16	HD_SEL
17	VD_SEL
18	VD_SEL
19	VD_SEL
20	GEN_IV
21	Reserved
22	MID
23	MID
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

FI RO, CON42[0], Alta

This bit indicates the current field index of the incoming video if the video is interlaced.

FI	Meaning
0	The field index is low
1	The field index is high

FIRST_FI R/W, CON42[1], Alta

This bit indicates the field index of the first field that was captured during a snap or grab operation.

FI	Meaning
0	The field index was low at the start of acquisition
1	The field index was high at the start of acquisition

RD_WEN R/W, CON42[2], Alta

This bit indicates the current status of the of the WEN I/O signal.

RD_HD	Meaning
0	The WEN input is currently low
1	The WEN input is currently high

RD_HD R/W, CON42[4], Alta

This bit indicates the current status of the of the horizontal sync (HD) I/O signal.

RD_HD	Meaning
0	The HD input is currently low
1	The HD input is currently high

RD_VD R/W, CON42[5], Alta

This bit indicates the current status of the of the vertical sync (HD) I/O signal.

RD_VD	Meaning
0	The VD input is currently low
1	The VD input is currently high

SWAP_LINES R/W, CON42[6], Alta

For some interlaced camera, the odd and even fields must be swapped.

SWAP_LINES	Meaning
0	Do not swap fields
1	Swap fields.

FI_POL R/W, CON42[7], Alta

Used to swap the polarity of the field index signal, needed for some interlaced cameras.

FI_POL	Meaning
0	Normal polarity
1	Invert polarity

SOE R/W, CON42[9..8], Alta

This bits dictates which field from an interlaced camera initiates acquisition.

SOE	Meaning
0	The odd field starts acquisition
1	The even field starts acquisition.

ACQ_IV R/W, CON42[10], Alta

This bit tells the acquisition engine if the board is acquiring interlaced or non-interlaced video.

ACQIV	Meaning
0	Incoming video is non-interlaced
1	Incoming video is interlaced

FEN_SEL R/W, CON42[13..11], Alta

This bitfield controls the sorce of the FEN signal used to control the acquisition engine..

FEN_SEL	Meaning
0 (000b)	Use VD signal from AFE
1 (001b)	Use WEN input signal
2 (010b)	Reserved
3 (011b)	Reserved
4 (100b)	Reserved
5 (101b)	Reserved
6 (110b)	Reserved
7 (111b)	Reserved

HD_SEL R/W, CON42[16..14], Alta

This bitfield controls the sorce of the HD output signal

HD_SEL	Meaning
0 (000b)	??
1 (001b)	HD is an output, source is this VFG"s Video Generator
2 (010b)	HD is an output, source is the master VFG"s Video Generator
3 (011b)	HD is an output, source the the CC3 signal

HD_SEL	Meaning
4 (100b)	HD is an output, source is the AFE's detected HD signal
5 (101b)	Reserved
6 (110b)	Reserved
7 (111b)	Reserved

VD_SEL R/W, CON42[19..17], Alta

This bitfield controls the sorce of the VD output signal.

VD_SEL	Meaning
0 (000b)	??
1 (001b)	VD is an output, source is this VFG"s Video Generator
2 (010b)	VD is an output, source is the master VFG"s Video Generator
3 (011b)	VD is an output, source the the CC4 signal
4 (100b)	VD is an output, source is the AFE's detected VD signal
5 (101b)	Reserved
6 (110b)	Reserved
7 (111b)	Reserved

GEN_IV R/W, CON42[20], Alta

This bit is used to select which video generator is used.

GEN_IV	Meaning
0	Standard video generator
1	Custom video generator

MID R/W, CON42[23..22], Alta

This bitfield is used to comminicate between multiple VFGs on the same board. What ever value is written to this register can be read from all the other VFGs. This register does not control anything.

5.37 CON43 Register

Bit	Name
0	GEN_H_PERIOD
1	GEN_H_PERIOD
2	GEN_H_PERIOD
3	GEN_H_PERIOD
4	GEN_H_PERIOD
5	GEN_H_PERIOD
6	GEN_H_PERIOD
7	GEN_H_PERIOD
8	GEN_H_PERIOD
9	GEN_H_PERIOD
10	GEN_H_PERIOD
11	GEN_H_PERIOD
12	GEN_H_PERIOD
13	GEN_H_PERIOD
14	GEN_H_PERIOD
15	GEN_H_PERIOD
16	GEN_H_LOW
17	GEN_H_LOW
18	GEN_H_LOW
19	GEN_H_LOW
20	GEN_H_LOW
21	GEN_H_LOW
22	GEN_H_LOW
23	GEN_H_LOW
24	GEN_H_LOW
25	GEN_H_LOW
26	GEN_H_LOW
27	GEN_H_LOW
28	GEN_H_LOW
29	GEN_H_LOW
30	GEN_H_LOW
31	GEN_H_LOW

GEN_H_PERIOD R/W, CON43[15..0], Alta

Horizontal period of Video Generator.

GEN_H_LOW R/W, CON43[15..0], Alta

Horizontal low period of Video Generator.

5.38 CON44 Register

Bit	Name
0	GEN_V_PERIOD
1	GEN_V_PERIOD
2	GEN_V_PERIOD
3	GEN_V_PERIOD
4	GEN_V_PERIOD
5	GEN_V_PERIOD
6	GEN_V_PERIOD
7	GEN_V_PERIOD
8	GEN_V_PERIOD
9	GEN_V_PERIOD
10	GEN_V_PERIOD
11	GEN_V_PERIOD
12	GEN_V_PERIOD
13	GEN_V_PERIOD
14	GEN_V_PERIOD
15	GEN_V_PERIOD
16	GEN_V_LOW
17	GEN_V_LOW
18	GEN_V_LOW
19	GEN_V_LOW
20	GEN_V_LOW
21	GEN_V_LOW
22	GEN_V_LOW
23	GEN_V_LOW
24	GEN_V_LOW
25	GEN_V_LOW
26	GEN_V_LOW
27	GEN_V_LOW
28	GEN_V_LOW
29	GEN_V_LOW
30	GEN_V_LOW
31	GEN_V_LOW

GEN_V_PERIOD R/W, CON43[15..0], Alta

Vertical period of Video Generator.

GEN_V_LOW R/W, CON43[15..0], Alta

Vertical low period of Video Generator.

5.39 CON51 Register

Bit	Name
0	QENC_COUNT
1	QENC_COUNT
2	QENC_COUNT
3	QENC_COUNT
4	QENC_COUNT
5	QENC_COUNT
6	QENC_COUNT
7	QENC_COUNT
8	QENC_COUNT
9	QENC_COUNT
10	QENC_COUNT
11	QENC_COUNT
12	QENC_COUNT
13	QENC_COUNT
14	QENC_COUNT
15	QENC_COUNT
16	QENC_COUNT
17	QENC_COUNT
18	QENC_COUNT
19	QENC_COUNT
20	QENC_COUNT
21	QENC_COUNT
22	QENC_COUNT
23	QENC_COUNT
24	QENC_PHASEA
25	QENC_PHASEB
26	QENC_DIR
27	QENC_INTRVL_IN
28	QENC_NEW_LINES
29	Reserved
30	Reserved
31	Reserved

QENC_COUNT RO, CON51[23..0], Karbon, Neon

This bitfield displays the current quadrature encoder count.

QENC_PHASEA RO, CON51[24], Karbon, Neon

This bit displays the current logic level of the A quadrature encoder phase.

QENC_PHASEB RO, CON51[25], Karbon, Neon

This bit displays the current logic level of the B quadrature encoder phase.

QENC_DIR RO, CON51[26], Karbon, Neon

This bit displays the current quadrature encoder direction.

QENC_DIR	Meaning
0	Direction is negative
1	Direction is positive

QENC_INTRVL_IN RO, CON51[27], Karbon, Neon

This bit indicates the current status of the quadrature encoder if the system is in interval mode (see QENC_INTRVL_MODE).

QENC_INTRVL_IN	Meaning
0	System is not inside the interval. Encoder counter is not between QENC_INTRVL_LL and QENC_INTRVL_UL. Lines are not being acquired.
1	System is inside the interval. Encoder counter is between QENC_INTRVL_LL and QENC_INTRVL_UL. Lines are being acquired.

QENC_NEW_LINES RO, CON51[28], Karbon, Neon

This bit indicates if the system is at an encoder count that corresponds to a new line. When QENC_NO_REAQ = 1, only lines that have not yet been scanned are acquired. This bit can be used to determine of new lines are being traversed, or if the system has backed up, and is revisiting old lines.

QENC_NEW_LINES	Meaning
0	The system is traversing lines that have already been visited. If QENC_NO_REAQ = 1, lines are not being acquired.
1	The system is traversing new lines. Lines are being acquired.

Analog Front End Registers

Chapter 6

6.1 Introduction

This section enumerates all of the bitfields in all of the registers used to control the analog front end (AFE) of the Alta. The AFE is a separate chip on the Alta which both digitizes the incoming video as well as produces the pixel clock (through its programmable PLL) used to drive the digital part of the board. The AFE is extremely flexible, as can be seen by the number of registers in this chapter. However, the tools available as part of the BitFlow SDK hide all the complication and let you make changes to these registers using a simple intuitive interface.

6.2 Bitfield definitions

6.2.1 Example Bitfield Definition

Here is what each bitfield definition looks like:

BITFIELD R/W, CON0[7..0], Alta, Karbon, Neon, R64

BitField discussion.

6.2.2 Bitfield Definition Explanation.

The definitions is broken into three sections (see Table 6-1).

Table 6-1 Bitfield Sections.

Section	Meaning
Bitfield name	This is the name of the bitfield. This name is use to program this bitfield from software or from within and camera configuration file. When programming bitfields from software using a Peek or Poke function, the bitfield is preceded with "REG_". For example the bitfield CFREQ is referred to in software as REG_CFREQ.
Bitfield details	This section describes how the bitfield is accessed. The first part describes the how the bits can be accessed. For example R/W means the register can be both read and writen. See theTable 6-2 for details.The second part is the wide register that the bitfield is located in. In the example above this bitfield is in CON0. Following the wide register name is a bitfield location description, in hardware engineering format. For example, [7..0], means the bitfield has 8 bits, location in positions 0 to 7. Finally this section also indicates if the register is specific to only one product family.
Bitfield discussion	This section explains the purposed of the bitfield in detail. Usually meaning of every possible value of the bitfield is listed.

Table 6-2 explains the abbreviations used in the bitfield definitions.

Table 6-2 Abbreviations

Access	Meaning
R/W	Bitfield can be read and written.
RO	Bitfield can only be read. Writing to this bit has no effect.
WO	Bitfield can only be written. Reading from this bit will return meaningless values.
Karbon	This bitfield is functional on the Karbon.
Neon	This bitfield is functional on the Neon
R64	This bitfield is functional on the R64 family.
Alta	This bitfield is functional on the Alta family.

6.3 AFE_DEVID

Bit	Name
0	DEV_REV
1	DEV_REV
2	DEV_REV
3	DEV_REV
4	DEV_ID
5	DEV_ID
6	DEV_ID
7	DEV_ID
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

DEV_REV RO, AFE_DEVID[3..0], Alta

Revision of the AFE.

DEV_ID RO, AFE_DEVID[7..4], Alta

Device ID of the AFE.

6.4 AFE_SYNC_STAT

Bit	Name
0	HSYNC1_ACTIVE
1	HSYNC2_ACTIVE
2	VSYNC1_ACTIVE
3	VSYNC2_ACTIVE
4	SOG1_ACTIVE
5	SOG2_ACTIVE
6	PLL_LOCKED
7	CSYNC_DETECTED
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

HSYNC1_ ACTIVE RO, AFE_SYNC_STAT[0], Alta

0: HSYNC1 is Inactive, 1: HSYNC1 is Active

HSYNC2_ ACTIVE RO, AFE_SYNC_STAT[1], Alta

0: HSYNC2 is Inactive, 1: HSYNC2 is Active

VSYNC1_ACTIVE RO, AFE_SYNC_STAT[2], Alta

0: VSYNC1 is Inactive, 1: VSYNC1 is Active

VSYNC2_ACTIVE RO, AFE_SYNC_STAT[3], Alta

0: VSYNC2 is Inactive, 1: VSYNC2 is Active

SOG1_ACTIVE RO, AFE_SYNC_STAT[4], Alta

0: SOG1 is Inactive, 1: SOG1 is Active

SOG2_ACTIVE RO, AFE_SYNC_STAT[5], Alta

0: SOG2 is Inactive, 1: SOG2 is Active

PLL_LOCKED RO, AFE_SYNC_STAT[6], Alta

0: PLL is unlocked, 1: PLL is locked to incoming HSYNC

CSYNC_ DETECTED RO, AFE_SYNC_STAT[7], Alta

0: Composite Sync signal not detected, 1: Composite Sync signal is detected

6.5 AFE_SYNC_POL

Bit	Name
0	HSYNC1_POL
1	HSYNC2_POL
2	VSYNC1_POL
3	VSYNC2_POL
4	HSYNC1_TRI_LEVEL
5	HSYNC2_TRI_LEVEL
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

HSYNC1_POL RO, AFE_SYNC_POL[0], Alta

0: HSYNC1 is Active High, 1: HSYNC1 is Active Low

HSYNC2_POL RO, AFE_SYNC_POL[1], Alta

0: HSYNC2 is Active High, 1: HSYNC2 is Active Low

VSYNC1_POL RO, AFE_SYNC_POL[2], Alta

0: VSYNC1 is Active High, 1: VSYNC1 is Active Low

VSYNC2_POL RO, AFE_SYNC_POL[3], Alta

0: VSYNC2 is Active High, 1: VSYNC2 is Active Low

HSYNC1_TRI_LEVEL RO, AFE_SYNC_POL[4], Alta

0: HSYNC1 is Standard Sync, 1: HSYNC1 is Trilevel Sync

HSYNC2_TRI_LEVEL RO, AFE_SYNC_POL[5], Alta

0: HSYNC2 is Standard Sync, 1: HSYNC2 is Trilevel Sync

6.6 AFE_HSYNC_SLICER

Bit	Name
0	HSYNC1_TRESH
1	HSYNC1_TRESH
2	HSYNC1_TRESH
3	Reserved
4	HSYNC2_TRESH
5	HSYNC2_TRESH
6	HSYNC2_TRESH
7	DISABLE_GLITCH
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

HSYNC1_TRESH R/W, AFE_HSYNC_SLICER[2..0], Alta

000 = lowest (0.4V) All values referred to, 011 = default (1.6V) voltage at HSYNC input, 111 = highest (3.2V) pin, 240mV hysteresis

HSYNC2_TRESH R/W, AFE_HSYNC_SLICER[6..4], Alta

See HSYNC1

DISABLE_ GLITCH R/W, AFE_HSYNC_SLICER[7], Alta

0: HSYNC/VSYNC Glitch Filter Enabled (default), 1: HSYNC/VSYNC Glitch Filter Disabled

6.7 AFE_SOG_SLICER

Bit	Name
0	SOG12_THRESH
1	SOG12_THRESH
2	SOG12_THRESH
3	SOG12_THRESH
4	SOG_FILTER
5	SOG_HYSTER_DIS
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

SOG12_THRESH R/W, AFE_SOG_SLICER[3..0], Alta

0x0 = lowest (0mV), 0x6 = default (120mV) 20mV step size, 0xF = highest (300mV)

SOG_FILTER R/W, AFE_SOG_SLICER[4], Alta

0: SOG low pass filter disabled, 1: SOG low pass filter enabled, 14MHz corner

SOG_HYSTER_DIS R/W, AFE_SOG_SLICER[5], Alta

0: 40mV SOG hysteresis enabled, 1: 40mV SOG hysteresis disabled (default)

6.8 AFE_IN_CNF

Bit	Name
0	CHAN_SEL
1	INPUT_COUPLING
2	YPBPR_INPUTS
3	SYNC_TYPE
4	COMP_SYNC_SRC
5	COAST_CLAMP_EN
6	SYNC_MASK_DIS
7	HSYNC_OUT_MASK_DIS
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

CHAN_SEL R/W, AFE_IN_CNF[0], Alta

0: VGA1, 1: VGA2

INPUT_COUPLING R/W, AFE_IN_CNF[1], Alta

0: AC coupled (positive input connected to clamp DAC, during clamp time, negative input disconnected from outside pad and always internally tied to appropriate clamp DAC). 1: DC coupled (+ and - inputs are brought to pads and never connected to clamp DACs). Analog clamp signal is turned off in this mode.

YPBPR_INPUTS R/W, AFE_IN_CNF[2], Alta

0: RGB inputs Base ABLC target code = 0x00 for R, G, and B), 1: YPbPr inputs Base ABLC target code = 0x00 for G (Y) Base ABLC target code = 0x80 for R (Pr) and B (Pb)

SYNC_TYPE R/W, AFE_IN_CNF[3], Alta

0: Separate HSYNC/VSYNC, 1: Composite (from SOG or CSYNC on HSYNC)

COMP_SYNC_SRC R/W, AFE_IN_CNF[4], Alta

0: SOGIN, 1: HSYNCIN

Note: If Sync Type = 0, the multiplexer will pass HSYNCIN regardless of the state of this bit.

COAST_CLAMP_EN R/W, AFE_IN_CNF[5], Alta

0: DC restore clamping and ABLC™ suspended, during COAST. 1: DC restore clamping and ABLC™ continue during COAST.

SYNC_MASK_DIS R/W, AFE_IN_CNF[6], Alta

0: Interval between HSYNC pulses masked (preventing PLL from seeing Macrovision and any spurious glitches). 1: Interval between HSYNC pulses not masked (Macrovision will cause PLL to lose lock).

HSYNC_OUT_MASK_DIS R/W, AFE_IN_CNF[7], Alta

0: HSYNCOUT signal is masked (any Macrovision, sync glitches on incoming SYNC are stripped from HSYNCOUT). 1: HSYNCOUT signal is not masked (any Macrovision, sync glitches on incoming SYNC appear on HSYNCOUT). If Sync Mask Disable = 1, HSYNCOUT is not masked.

6.9 AFE_RED_GAIN

Bit	Name
0	RED_CHAN_GAIN
1	RED_CHAN_GAIN
2	RED_CHAN_GAIN
3	RED_CHAN_GAIN
4	RED_CHAN_GAIN
5	RED_CHAN_GAIN
6	RED_CHAN_GAIN
7	RED_CHAN_GAIN
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

RED_CHAN_GAIN R/W, AFE_RED_GAIN[7..0], Alta

Red Channel Gain. Where gain (V/V) = 0.5 + RED_CHAN_GAIN/170

0x00: gain = 0.5V/V (1.4VP-P input = full range of ADC)
0x55: gain = 1.0V/V (0.7VP-P input = full range of ADC
0xFF: gain = 2.0V/V (0.35VP-P input = full range of ADC)

6.10 AFE_GREEN_GAIN

Bit	Name
0	GREEN_CHAN_GAIN
1	GREEN_CHAN_GAIN
2	GREEN_CHAN_GAIN
3	GREEN_CHAN_GAIN
4	GREEN_CHAN_GAIN
5	GREEN_CHAN_GAIN
6	GREEN_CHAN_GAIN
7	GREEN_CHAN_GAIN
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

GREEN_CHAN_GAIN R/W, AFE_GREEN_GAIN[7..0], Alta

Green/Monochrome Channel Gain. Where gain (V/V) = 0.5 + GREEN_CHAN_GAIN/170

0x00: gain = 0.5V/V (1.4VP-P input = full range of ADC)
0x55: gain = 1.0V/V (0.7VP-P input = full range of ADC
0xFF: gain = 2.0V/V (0.35VP-P input = full range of ADC)

6.11 AFE_BLUE_GAIN

Bit	Name
0	BLUE_CHAN_GAIN
1	BLUE_CHAN_GAIN
2	BLUE_CHAN_GAIN
3	BLUE_CHAN_GAIN
4	BLUE_CHAN_GAIN
5	BLUE_CHAN_GAIN
6	BLUE_CHAN_GAIN
7	BLUE_CHAN_GAIN
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

BLUE_CHAN_GAIN R/W, AFE_BLUE_GAIN[7..0], Alta

Blue Channel Gain. Where gain (V/V) = 0.5 +BLUE_CHAN_GAIN/170

0x00: gain = 0.5V/V (1.4VP-P input = full range of ADC)
0x55: gain = 1.0V/V (0.7VP-P input = full range of ADC
0xFF: gain = 2.0V/V (0.35VP-P input = full range of ADC)

6.12 AFE_RED_OFFS

Bit	Name
0	RED_CHAN_OFFSET
1	RED_CHAN_OFFSET
2	RED_CHAN_OFFSET
3	RED_CHAN_OFFSET
4	RED_CHAN_OFFSET
5	RED_CHAN_OFFSET
6	RED_CHAN_OFFSET
7	RED_CHAN_OFFSET
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

RED_CHAN_ OFFSET

R/W, AFE_RED_OFFS[7..0], Alta

ABLC™ enabled: digital offset control. A 1LSB change in this register will shift the ADC output by 1 LSB. ABLC™ disabled: analog offset control. These bits go to the upper 8-bits of the 10-bit offset DAC. A 1LSB change in this register will shift the ADC output approximately 1 LSB (Offset DAC range = 0) or 0.5LSBs (Offset DAC range = 1).

0x00 = min DAC value or -0x80 digital offset
0x80 = mid DAC value or 0x00 digital offset
0xFF = max DAC value or +0x7F digital offset

6.13 AFE_GREEN_OFFS

Bit	Name
0	GREEN_CHAN_OFFSET
1	GREEN_CHAN_OFFSET
2	GREEN_CHAN_OFFSET
3	GREEN_CHAN_OFFSET
4	GREEN_CHAN_OFFSET
5	GREEN_CHAN_OFFSET
6	GREEN_CHAN_OFFSET
7	GREEN_CHAN_OFFSET
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

GREEN_CHAN_OFFSET R/W, AFE_GREEN_OFFS[7..0], Alta

ABLC™ enabled: digital offset control. A 1LSB change in this register will shift the ADC output by 1 LSB. ABLC™ disabled: analog offset control. These bits go to the upper 8-bits of the 10-bit offset DAC. A 1LSB change in this register will shift the ADC output approximately 1 LSB (Offset DAC range = 0) or 0.5LSBs (Offset DAC range = 1).

0x00 = min DAC value or -0x80 digital offset
0x80 = mid DAC value or 0x00 digital offset
0xFF = max DAC value or +0x7F digital offset

6.14 AFE_BLUE_OFFS

Bit	Name
0	BLUE_CHAN_OFFSET
1	BLUE_CHAN_OFFSET
2	BLUE_CHAN_OFFSET
3	BLUE_CHAN_OFFSET
4	BLUE_CHAN_OFFSET
5	BLUE_CHAN_OFFSET
6	BLUE_CHAN_OFFSET
7	BLUE_CHAN_OFFSET
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

BLUE_CHAN_OFFSET R/W, AFE_BLUE_OFFS[7..0], Alta

ABLC™ enabled: digital offset control. A 1LSB change in this register will shift the ADC output by 1 LSB. ABLC™ disabled: analog offset control. These bits go to the upper 8-bits of the 10-bit offset DAC. A 1LSB change in this register will shift the ADC output approximately 1 LSB (Offset DAC range = 0) or 0.5LSBs (Offset DAC range = 1).

0x00 = min DAC value or -0x80 digital offset
0x80 = mid DAC value or 0x00 digital offset
0xFF = max DAC value or +0x7F digital offset

6.15 AFE_OFFS_DAC_CNF

Bit	Name
0	OFFSET_DAC_RANGE
1	Reserved
2	RED_OFFSET_DAC_LSB
3	RED_OFFSET_DAC_LSB
4	GREEN_OFFSET_DAC_LSB
5	GREEN_OFFSET_DAC_LSB
6	BLUE_OFFSET_DAC_LSB
7	BLUE_OFFSET_DAC_LSB
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

OFFSET_DAC_RANGE R/W, AFE_OFFS_DAC_CNF[0], Alta

0: ±½ ADC full scale (1 DAC LSB ~ 1 ADC LSB) 1: ±¼ ADC full scale (1 DAC LSB ~ ½ ADC LSB)

RED_OFFSET_DAC_LSB R/W, AFE_OFFS_DAC_CNF[3..2], Alta

These bits are the LSBs necessary for 10-bit manual offset DAC control. Combine with RED_CHAN_OFFSET to achieve 10-bit offset DAC control.

GREEN_OFFSET_DAC_LSB R/W, AFE_OFFS_DAC_CNF[5..4], Alta

These bits are the LSBs necessary for 10-bit manual offset DAC control. Combine with GREEN_CHAN_OFFSET to achieve 10-bit offset DAC control.

BLUE_OFFSET_DAC_LSB R/W, AFE_OFFS_DAC_CNF[7..6], Alta

These bits are the LSBs necessary for 10-bit manual offset DAC control. Combine with BLUE_CHAN_OFFSET to achieve 10-bit offset DAC control.

6.16 AFE_BANDWIDTH

Bit	Name
0	BANDWIDTH
1	BANDWIDTH
2	BANDWIDTH
3	BANDWIDTH
4	PEAKING
5	PEAKING
6	PEAKING
7	PEAKING
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

BANDWIDTH R/W, AFE_BANDWIDTH[3..0], Alta

3dB point for AFE lowpass filter 000b: 100MHz 111b: 780MHz (default)

PEAKING R/W, AFE_BANDWIDTH[7..4], Alta

0x0: Peaking off 0x1: Moderate peaking 0x2: Maximum recommended peaking (default). Values above 2 are not recommended.

6.17 AFE_PLL_HTOTAL_MSB

Bit	Name
0	PLL_H_TOTAL_MSB
1	PLL_H_TOTAL_MSB
2	PLL_H_TOTAL_MSB
3	PLL_H_TOTAL_MSB
4	PLL_H_TOTAL_MSB
5	PLL_H_TOTAL_MSB
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

PLL_H_TOTAL_MSB R/W, AFE_PLL_HTOTAL_MSB[5..0], Alta

This is the 5 MSB of HTOTAL (number of active pixels) value The minimum HTOTAL value supported is 0x200.

6.18 AFE_PLL_HTOTAL_LSB

Bit	Name
0	PLL_H_TOTAL_LSB
1	PLL_H_TOTAL_LSB
2	PLL_H_TOTAL_LSB
3	PLL_H_TOTAL_LSB
4	PLL_H_TOTAL_LSB
5	PLL_H_TOTAL_LSB
6	PLL_H_TOTAL_LSB
7	PLL_H_TOTAL_LSB
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

PLL_H_TOTAL_LSB R/W, AFE_PLL_HTOTAL_LSB[7..0], Alta

This is the 7 LSB of HTOTAL (number of active pixels) value The minimum HTOTAL value supported is 0x200.

6.19 AFE_PLL_SAMPLE_PHASE

Bit	Name
0	PLL_SAMPLE_PHASE
1	PLL_SAMPLE_PHASE
2	PLL_SAMPLE_PHASE
3	PLL_SAMPLE_PHASE
4	PLL_SAMPLE_PHASE
5	PLL_SAMPLE_PHASE
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

PLL_SAMPLE_PHASE R/W, AFE_PLL_SAMPLE_PHASE[5..0], Alta

PLL Sampling Phase Used to control the phase of the ADC's sample point relative to the period of a pixel. Adjust to obtain optimum image quality. One step = 5.625° (1.56% of pixel period).

6.20 AFE_PLL_PRE_COAST

Bit	Name
0	PLL_PRE_COAST
1	PLL_PRE_COAST
2	PLL_PRE_COAST
3	PLL_PRE_COAST
4	PLL_PRE_COAST
5	PLL_PRE_COAST
6	PLL_PRE_COAST
7	PLL_PRE_COAST
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

PLL_PRE_COAST R/W, AFE_PLL_PRE_COAST[7..0], Alta

Number of lines the PLL will coast prior to the start of VSYNC.

6.21 AFE_PLL_POST_COAST

Bit	Name
0	PLL_POST_COAST
1	PLL_POST_COAST
2	PLL_POST_COAST
3	PLL_POST_COAST
4	PLL_POST_COAST
5	PLL_POST_COAST
6	PLL_POST_COAST
7	PLL_POST_COAST
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

PLL_POST_COAST R/W, AFE_PLL_POST_COAST[7..0], Alta

Number of lines the PLL will coast after the start of VSYNC.

6.22 AFE_PLL_MISC

Bit	Name
0	PLL_HSYNC1_LOCK_EDGE
1	Reserved
2	PLL_HSYNC2_LOCK_EDGE
3	CLKINV_IN_PIN_DIS
4	CLKINV_IN_PIN_FUNC
5	CLKINV_IN_PIN_FUNC
6	XCLK_OUT_FREQ
7	XCLK_OUT_DIS
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

PLL_HSYNC1_LOCK_EDGE R/W, AFE_PLL_MISC[0], Alta

0: Lock on trailing edge of HSYNC1 (default), 1: Lock on leading edge of HSYNC1.

PLL_HSYNC2_LOCK_EDGE R/W, AFE_PLL_MISC[2], Alta

0: Lock on trailing edge of HSYNC2 (default), 1: Lock on leading edge of HSYNC2.

CLKINV_IN_PIN_DIS R/W, AFE_PLL_MISC[3], Alta

0: CLKINVIN pin enabled (default) 1: CLKINVIN pin disabled (internally forced low).

CLKINV_IN_PIN_FUNC R/W, AFE_PLL_MISC[5..4], Alta

00: CLKINV (default), 01: External CLAMP (See Note), 10: External COAST, 11: External PIXCLK.

Note: the CLAMP pulse is used to:

Perform a DC restore (if enabled)
Start the ABLC™ function (if enabled)
update the data to the Offset DACs (always).

In the default internal CLAMP mode, the ISL98001 automatically generates the CLAMP pulse. If External CLAMP is selected, the Offset DAC values only change on the leading edge of CLAMP. If there is no internal clamp signal, there will be up to a 100ms delay between when the PGA gain or offset DAC register is written to, and when the PGA or offset DAC is actually updated.

XCLK_OUT_FREQ R/W, AFE_PLL_MISC[6], Alta

0: XCLKOUT = fCRYSTAL (default), 1: XCLKOUT = fCRYSTAL/2.

XCLK_OUT_DIS R/W, AFE_PLL_MISC[7], Alta

0 = XCLKOUT enabled, 1 = XCLKOUT is logic low

6.23 AFE_DC_RSTR_PIX_MSB

Bit	Name
0	DC_RSTR_PIX_MSB
1	DC_RSTR_PIX_MSB
2	DC_RSTR_PIX_MSB
3	DC_RSTR_PIX_MSB
4	DC_RSTR_PIX_MSB
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

DC_RSTR_PIX_MSB R/W, AFE_DC_RSTR_PIX_MSB[4..0], Alta

This is the 5 MSBs of the DC_RSTR_PIX.Pixel after HSYNCIN trailing edge to begin DC restore and ABLC™ functions. 13-bits. Set this register to the first stable black pixel following the trailing edge of HSYNCIN.

6.24 AFE_DC_RSTR_PIX_LSB

Bit	Name
0	DC_RSTR_PIX_LSB
1	DC_RSTR_PIX_LSB
2	DC_RSTR_PIX_LSB
3	DC_RSTR_PIX_LSB
4	DC_RSTR_PIX_LSB
5	DC_RSTR_PIX_LSB
6	DC_RSTR_PIX_LSB
7	DC_RSTR_PIX_LSB
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

DC_RSTR_PIX_LSB R/W, AFE_DC_RSTR_PIX_LSB[7..0], Alta

This is the 8 LSBs of the DC_RSTR_PIX. Pixel after HSYNCIN trailing edge to begin DC restore and ABLC™ functions. 13-bits. Set this register to the first stable black pixel following the trailing edge of HSYNCIN.

6.25 AFE_DC_RSTR_WIDTH

Bit	Name
0	DC_REST_CLAMP_WIDTH
1	DC_REST_CLAMP_WIDTH
2	DC_REST_CLAMP_WIDTH
3	DC_REST_CLAMP_WIDTH
4	DC_REST_CLAMP_WIDTH
5	DC_REST_CLAMP_WIDTH
6	DC_REST_CLAMP_WIDTH
7	DC_REST_CLAMP_WIDTH
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

DC_REST_CLAMP_WIDTH R/W, AFE_DC_RSTR_WIDTH[7..0], Alta

Width of DC restore clamp used in AC-coupled configurations. Has no effect on ABLC™. Minimum value is 0x02 (a setting of 0x01 or 0x00 will not generate a clamp pulse).

6.26 AFE_ABLC_CNF

Bit	Name
0	ABLC_DIS
1	Reserved
2	ABLC_PIX_WIDTH
3	ABLC_PIX_WIDTH
4	ABLC_BANDWIDTH
5	ABLC_BANDWIDTH
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

ABLC_DIS R/W, AFE_ABLC_CNF[0], Alta

0: ABLC™ enabled (default), 1: ABLC™ disabled.

ABLC_PIX_WIDTH R/W, AFE_ABLC_CNF[3..2], Alta

Number of black pixels averaged every line for ABLC™ function.

00: 16 pixels [default]
01: 32 pixels
10: 64 pixels
11: 128 pixels

ABLC_BANDWIDTH R/W, AFE_ABLC_CNF[5..4], Alta

Time constant (lines) = 2(5+[6:4]).

000 = 32 lines
100 = 512 lines (default
111 = 4096 lines

6.27 AFE_OUT_FORMAT

Bit	Name
0	OUT_BUS_WIDTH
1	OUT_INTERLEAVE
2	OUT_BUS_SWAP
3	OUT_UV_ORDER
4	OUT_422_MODE
5	DATACLK_POL
6	VSOUT_POL
7	HSOUT_POL
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

OUT_BUS_WIDTH R/W, AFE_OUT_FORMAT[0], Alta

0: 24-bits: Data output on RP, GP, BP only; RS, GS, BS are all driven low (default). 1: 48-bits: Data output on RP, RS, GP, GS, BP, BS.

OUT_INTERLEAVE R/W, AFE_OUT_FORMAT[1], Alta

0: No interleaving: data changes on same edge of DATACLK (default). 1: Interleaved: Secondary data bus data changes on opposite edge of DATACLK from primary data-bus.

OUT_BUS_SWAP R/W, AFE_OUT_FORMAT[2], Alta

0: First data byte after trailing edge of HSOUT appears on RP, GP, BP (default). 1: First data byte after trailing edge of HSOUT appears on RS, GS, BS (primary and secondary busses are reversed).

OUT_UV_ORDER R/W, AFE_OUT_FORMAT[3], Alta

0: U0 V0 U2 V2 U4 V4 U6 V6… (default), 1: U0 V1 U2 V3 U4 V5 U6 V7… (X980xx).

OUT_422_MODE R/W, AFE_OUT_FORMAT[4], Alta

1: Data is decimated to 4:2:2 (YUV), blue channel is driven low.

DATACLK_POL R/W, AFE_OUT_FORMAT[5], Alta

0: HSOUT, VSOUT, and Pixel Data changes on falling edge of DATACLK (default). 1: HSOUT, VSOUT, and Pixel Data changes on rising edge of DATACLK.

VSOUT_POL R/W, AFE_OUT_FORMAT[6], Alta

0: Active High (default), 1: Active Low.

HSOUT_POL R/W, AFE_OUT_FORMAT[7], Alta

0: Active High (default), 1: Active Low.

6.28 AFE_HSOUT_WIDTH

Bit	Name
0	HSOUT_WIDTH
1	HSOUT_WIDTH
2	HSOUT_WIDTH
3	HSOUT_WIDTH
4	HSOUT_WIDTH
5	HSOUT_WIDTH
6	HSOUT_WIDTH
7	HSOUT_WIDTH
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

HSOUT_WIDTH R/W, AFE_HSOUT_WIDTH[7..0], Alta

HSOUT width, in pixels. Minimum value is 0x01 for 24-bit modes, 0x02 for 48-bit modes.

6.29 AFE_OUT_SIG_DISABLE

Bit	Name
0	RP_OUT_TRI
1	RS_OUT_TRI
2	GP_OUT_TRI
3	GS_OUT_TRI
4	BP_OUT_TRI
5	BS_OUT_TRI
6	DATACLK_NOT_TRI
7	DATACLK_TRI
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

RP_OUT_TRI R/W, AFE_OUT_SIG_DISABLE[0], Alta

0 = Output byte enabled 1 = Output byte three-stated These bits override all other I/O settings Output data pins have 56k Ohm pulldown resistors to GNDD.

RS_OUT_TRI R/W, AFE_OUT_SIG_DISABLE[1], Alta

0 = Output byte enabled 1 = Output byte three-stated These bits override all other I/O settings Output data pins have 56k Ohm pulldown resistors to GNDD.

GP_OUT_TRI R/W, AFE_OUT_SIG_DISABLE[2], Alta

0 = Output byte enabled 1 = Output byte three-stated These bits override all other I/O settings Output data pins have 56k Ohm pulldown resistors to GNDD.

GS_OUT_TRI R/W, AFE_OUT_SIG_DISABLE[3], Alta

0 = Output byte enabled 1 = Output byte three-stated These bits override all other I/O settings Output data pins have 56k Ohm pulldown resistors to GNDD.

BP_OUT_TRI R/W, AFE_OUT_SIG_DISABLE[4], Alta

0 = Output byte enabled 1 = Output byte three-stated These bits override all other I/O settings Output data pins have 56k Ohm pulldown resistors to GNDD.

BS_OUT_TRI R/W, AFE_OUT_SIG_DISABLE[5], Alta

0 = Output byte enabled 1 = Output byte three-stated These bits override all other I/O settings Output data pins have 56k Ohm pulldown resistors to GNDD.

DATACLK_NOT_TRI R/W, AFE_OUT_SIG_DISABLE[6], Alta

0 = DATACLK enabled 1 = DATACLK three-stated.

DATACLK_TRI R/W, AFE_OUT_SIG_DISABLE[7], Alta

0 = DATACLK enabled 1 = DATACLK three-stated.

6.30 AFE_POWER_CON

Bit	Name
0	RED_PWR_DOWN
1	GREEN_PWR_DOWN
2	BLUE_PWR_DOWN
3	PLL_PWR_DOWN
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

RED_PWR_DOWN R/W, AFE_POWER_CON[0], Alta

0 = Red ADC operational (default), 1 = Red ADC powered down.

GREEN_PWR_DOWN R/W, AFE_POWER_CON[1], Alta

0 = Green ADC operational (default), 1 = Green ADC powered down.

BLUE_PWR_DOWN R/W, AFE_POWER_CON[2], Alta

0 = Blue ADC operational (default), 1 = Blue ADC powered down.

PLL_PWR_DOWN R/W, AFE_POWER_CON[3], Alta

0 = PLL operational (default), 1 = PLL powered down.

6.31 AFE_PLL_TUNING

Bit	Name
0	PLL_TUNING
1	PLL_TUNING
2	PLL_TUNING
3	PLL_TUNING
4	PLL_TUNING
5	PLL_TUNING
6	PLL_TUNING
7	PLL_TUNING
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

PLL_TUNING R/W, AFE_PLL_TUNING[7..0], Alta

Use default setting of 0x49 for all PC and video modes except signals coming from an analog VCR. Set to 0x4C for analog videotape compatibility.

6.32 AFE_RED_ABLC

Bit	Name
0	RED_ABLC_TARGET
1	RED_ABLC_TARGET
2	RED_ABLC_TARGET
3	RED_ABLC_TARGET
4	RED_ABLC_TARGET
5	RED_ABLC_TARGET
6	RED_ABLC_TARGET
7	RED_ABLC_TARGET
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

RED_ABLC_ TARGET

R/W, AFE_RED_ABLC[7..0], Alta

This is a 2's complement number controlling the target code of the Red ADC output when ABLC is enabled. In RGB mode, the Red ADC output will be servoed to 0x00 + the number in this register (-0x00 to +0x7F). In YPbPr mode, the Red ADC output will be servoed to 0x80 + the number in this register (-0x80 to +0x7F). Note: This register does NOT disable the digital offset adder. Both functions can be used simultaneously.

6.33 AFE_GREEN_ABLC

Bit	Name
0	GREEN_ABLC_TARGET
1	GREEN_ABLC_TARGET
2	GREEN_ABLC_TARGET
3	GREEN_ABLC_TARGET
4	GREEN_ABLC_TARGET
5	GREEN_ABLC_TARGET
6	GREEN_ABLC_TARGET
7	GREEN_ABLC_TARGET
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

GREEN_ABLC_TARGET R/W, AFE_GREEN_ABLC[7..0], Alta

This is a 2's complement number controlling the target code of the Green ADC output when ABLC is enabled. In RGB and YPbPr modes, the Green ADC output will be servoed to 0x00 + the number in this register (-0x00 to +0x7F). Note: This register does NOT disable the digital offset adder. Both functions can be used simultaneously.

6.34 AFE_BLUE_ABLC

Bit	Name
0	BLUE_ABLC_TARGET
1	BLUE_ABLC_TARGET
2	BLUE_ABLC_TARGET
3	BLUE_ABLC_TARGET
4	BLUE_ABLC_TARGET
5	BLUE_ABLC_TARGET
6	BLUE_ABLC_TARGET
7	BLUE_ABLC_TARGET
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

BLUE_ABLC_TARGET R/W, AFE_BLUE_ABLC[7..0], Alta

This is a 2's complement number controlling the target code of the Blue ADC output when ABLC is enabled. In RGB mode, the Blue ADC output will be servoed to 0x00 + the number in this register (-0x00 to +0x7F). In YPbPr mode, the Blue ADC output will be servoed to 0x80 + the number in this register (-0x80 to +0x7F). Note: This register does NOT disable the digital offset adder. Both functions can be used simultaneously.

6.35 AFE_DC_RSTR_CLAMP

Bit	Name
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	DC_RSTR_CLAMP_IMP
5	DC_RSTR_CLAMP_IMP
6	DC_RSTR_CLAMP_IMP
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

DC_RSTR_CLAMP_IMP R/W, AFE_DC_RSTR_CLAMP[6..4], Alta

DC Restore clamp's ON resistance. Shared for all three channels:

0: Infinite (clamp disconnected) (default)
1: 1600 Ohm
2: 800 Ohm
3: 533 Ohm
4: 400 Ohm
5: 320 Ohm
6: 267 Ohm
7: 228 Ohm

6.36 AFE_SYNC_SEP_CON

Bit	Name
0	OUT_SYNC_TRI
1	COAST_POL
2	HSOUT_LOCK_EDGE
3	Reserved
4	VSYNCOUT_MODE
5	Reserved
6	Reserved
7	VSOUT_MODE
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

OUT_SYNC_TRI R/W, AFE_SYNC_SEP_CON[0], Alta

0: VSYNCOUT, HSYNCOUT, VSOUT, HSOUT are active (default). 1: VSYNCOUT, HSYNCOUT, VSOUT, HSOUT are in three-state.

COAST_POL R/W, AFE_SYNC_SEP_CON[1], Alta

0: Coast active high (default), 1: Coast active low Set to 0 for internal VSYNC extracted from CSYNC. Set to 0 or 1 as appropriate to match external VSYNC or external COAST.

HSOUT_LOCK_EDGE R/W, AFE_SYNC_SEP_CON[2], Alta

0: HSOUT's trailing edge is locked to selected HSYNCIN's lock edge. Leading edge moves backward in time as HSOUT width is increased (X980xx default). 1: HSOUT's leading edge is locked to selected HSYNCIN's lock edge. Trailing edge moves forward in time as HSOUT width is increased.

VSYNCOUT_MODE R/W, AFE_SYNC_SEP_CON[4], Alta

0: VSYNCOUT is aligned to HSYNCOUT edge, providing “perfect” VSYNC signal (default). 1: VSYNCOUT is “raw” integrator output.

VSOUT_MODE R/W, AFE_SYNC_SEP_CON[7], Alta

0: VSOUT is output on VSOUT pin (default). 1: COAST (including pre- and post-coast COAST) is output on VSOUT pin.

Karbon/Neon/Alta DMA

Chapter 7

7.1 Introduction

This section enumerates all of the registers that control DMA on boards using the PLDA DMA engine. This includes the Alta, the Karbon and the Neon families. This chapter also covers the scatter gather DMA instructions (Quads or QTabs). The formatting of the register sections is explained in Section 5.2.

7.2 CON28 Register

Bit	Name
0	FIRST_QUAD_PTR_LO
1	FIRST_QUAD_PTR_LO
2	FIRST_QUAD_PTR_LO
3	FIRST_QUAD_PTR_LO
4	FIRST_QUAD_PTR_LO
5	FIRST_QUAD_PTR_LO
6	FIRST_QUAD_PTR_LO
7	FIRST_QUAD_PTR_LO
8	FIRST_QUAD_PTR_LO
9	FIRST_QUAD_PTR_LO
10	FIRST_QUAD_PTR_LO
11	FIRST_QUAD_PTR_LO
12	FIRST_QUAD_PTR_LO
13	FIRST_QUAD_PTR_LO
14	FIRST_QUAD_PTR_LO
15	FIRST_QUAD_PTR_LO
16	FIRST_QUAD_PTR_LO
17	FIRST_QUAD_PTR_LO
18	FIRST_QUAD_PTR_LO
19	FIRST_QUAD_PTR_LO
20	FIRST_QUAD_PTR_LO
21	FIRST_QUAD_PTR_LO
22	FIRST_QUAD_PTR_LO
23	FIRST_QUAD_PTR_LO
24	FIRST_QUAD_PTR_LO
25	FIRST_QUAD_PTR_LO
26	FIRST_QUAD_PTR_LO
27	FIRST_QUAD_PTR_LO
28	FIRST_QUAD_PTR_LO
29	FIRST_QUAD_PTR_LO
30	FIRST_QUAD_PTR_LO
31	FIRST_QUAD_PTR_LO

FIRST_QUAD_PTR_LO R/W, CON28[31..0], Alta, Karbon, Neon

This is the low word of the 64-bit address of the first DMA scatter-gather instruction in a chain of instructions. This register can be written at any time, but the DMA engine only loads this value when byte count (as set by CHAIN_DATA_SIZE_LO/CHAIN_DATA_SIZE_HI) goes to zero.

7.3 CON29 Register

Bit	Name
0	FIRST_QUAD_PTR_HI
1	FIRST_QUAD_PTR_HI
2	FIRST_QUAD_PTR_HI
3	FIRST_QUAD_PTR_HI
4	FIRST_QUAD_PTR_HI
5	FIRST_QUAD_PTR_HI
6	FIRST_QUAD_PTR_HI
7	FIRST_QUAD_PTR_HI
8	FIRST_QUAD_PTR_HI
9	FIRST_QUAD_PTR_HI
10	FIRST_QUAD_PTR_HI
11	FIRST_QUAD_PTR_HI
12	FIRST_QUAD_PTR_HI
13	FIRST_QUAD_PTR_HI
14	FIRST_QUAD_PTR_HI
15	FIRST_QUAD_PTR_HI
16	FIRST_QUAD_PTR_HI
17	FIRST_QUAD_PTR_HI
18	FIRST_QUAD_PTR_HI
19	FIRST_QUAD_PTR_HI
20	FIRST_QUAD_PTR_HI
21	FIRST_QUAD_PTR_HI
22	FIRST_QUAD_PTR_HI
23	FIRST_QUAD_PTR_HI
24	FIRST_QUAD_PTR_HI
25	FIRST_QUAD_PTR_HI
26	FIRST_QUAD_PTR_HI
27	FIRST_QUAD_PTR_HI
28	FIRST_QUAD_PTR_HI
29	FIRST_QUAD_PTR_HI
30	FIRST_QUAD_PTR_HI
31	FIRST_QUAD_PTR_HI

FIRST_QUAD_PTR_HI R/W, CON29[31..0], Alta, Karbon, Neon

This is the high word of the 64-bit address of the first DMA scatter-gather instruction in a chain of instructions. This register can be written at any time, but the DMA engine only loads this value when byte count (as set by CHAIN_DATA_SIZE_LO/CHAIN_DATA_SIZE_HI) goes to zero.

7.4 CON30 Register

Bit	Name
0	CHAIN_DATA_SIZE_LO
1	CHAIN_DATA_SIZE_LO
2	CHAIN_DATA_SIZE_LO
3	CHAIN_DATA_SIZE_LO
4	CHAIN_DATA_SIZE_LO
5	CHAIN_DATA_SIZE_LO
6	CHAIN_DATA_SIZE_LO
7	CHAIN_DATA_SIZE_LO
8	CHAIN_DATA_SIZE_LO
9	CHAIN_DATA_SIZE_LO
10	CHAIN_DATA_SIZE_LO
11	CHAIN_DATA_SIZE_LO
12	CHAIN_DATA_SIZE_LO
13	CHAIN_DATA_SIZE_LO
14	CHAIN_DATA_SIZE_LO
15	CHAIN_DATA_SIZE_LO
16	CHAIN_DATA_SIZE_LO
17	CHAIN_DATA_SIZE_LO
18	CHAIN_DATA_SIZE_LO
19	CHAIN_DATA_SIZE_LO
20	CHAIN_DATA_SIZE_LO
21	CHAIN_DATA_SIZE_LO
22	CHAIN_DATA_SIZE_LO
23	CHAIN_DATA_SIZE_LO
24	CHAIN_DATA_SIZE_LO
25	CHAIN_DATA_SIZE_LO
26	CHAIN_DATA_SIZE_LO
27	CHAIN_DATA_SIZE_LO
28	CHAIN_DATA_SIZE_LO
29	CHAIN_DATA_SIZE_LO
30	CHAIN_DATA_SIZE_LO
31	CHAIN_DATA_SIZE_LO

CHAIN_DATA_SIZE_LO R/W, CON30[31..0], Alta, Karbon, Neon

This is the low word if the low word of the 64-bit number of bytes in the chain. The value in this register is loaded into the DMA engine when DMA is initiated. This value is then decremented every DMA transfer. When the count reached zero, this value in this register is reloaded into the DMA engine, and the first scatter gather instruction pointed to by FIRST_QUAD_PTR_HI and FIRST_QUAD_PTR_LO is loaded.

7.5 CON31 Register

Bit	Name
0	CHAIN_DATA_SIZE_HI
1	CHAIN_DATA_SIZE_HI
2	CHAIN_DATA_SIZE_HI
3	CHAIN_DATA_SIZE_HI
4	CHAIN_DATA_SIZE_HI
5	CHAIN_DATA_SIZE_HI
6	CHAIN_DATA_SIZE_HI
7	CHAIN_DATA_SIZE_HI
8	CHAIN_DATA_SIZE_HI
9	CHAIN_DATA_SIZE_HI
10	CHAIN_DATA_SIZE_HI
11	CHAIN_DATA_SIZE_HI
12	CHAIN_DATA_SIZE_HI
13	CHAIN_DATA_SIZE_HI
14	CHAIN_DATA_SIZE_HI
15	CHAIN_DATA_SIZE_HI
16	CHAIN_DATA_SIZE_HI
17	CHAIN_DATA_SIZE_HI
18	CHAIN_DATA_SIZE_HI
19	CHAIN_DATA_SIZE_HI
20	CHAIN_DATA_SIZE_HI
21	CHAIN_DATA_SIZE_HI
22	CHAIN_DATA_SIZE_HI
23	CHAIN_DATA_SIZE_HI
24	CHAIN_DATA_SIZE_HI
25	CHAIN_DATA_SIZE_HI
26	CHAIN_DATA_SIZE_HI
27	CHAIN_DATA_SIZE_HI
28	CHAIN_DATA_SIZE_HI
29	CHAIN_DATA_SIZE_HI
30	CHAIN_DATA_SIZE_HI
31	CHAIN_DATA_SIZE_HI

CHAIN_DATA_SIZE_HI R/W, CON31[31..0], Alta, Karbon, Neon

This is the high word if the 64-bit number bytes in the chain. The value in this register is loaded into the DMA engine when DMA is initiated. This value is then decremented every DMA transfer. When the count reached zero, this value in this register is reloaded into the DMA engine, and the first scatter gather instruction pointed to by FIRST_QUAD_PTR_HI and FIRST_QUAD_PTR_LO is loaded.

7.6 CON32 Register

Bit	Name
0	CHAIN_DATA_TOGO_LO
1	CHAIN_DATA_TOGO_LO
2	CHAIN_DATA_TOGO_LO
3	CHAIN_DATA_TOGO_LO
4	CHAIN_DATA_TOGO_LO
5	CHAIN_DATA_TOGO_LO
6	CHAIN_DATA_TOGO_LO
7	CHAIN_DATA_TOGO_LO
8	CHAIN_DATA_TOGO_LO
9	CHAIN_DATA_TOGO_LO
10	CHAIN_DATA_TOGO_LO
11	CHAIN_DATA_TOGO_LO
12	CHAIN_DATA_TOGO_LO
13	CHAIN_DATA_TOGO_LO
14	CHAIN_DATA_TOGO_LO
15	CHAIN_DATA_TOGO_LO
16	CHAIN_DATA_TOGO_LO
17	CHAIN_DATA_TOGO_LO
18	CHAIN_DATA_TOGO_LO
19	CHAIN_DATA_TOGO_LO
20	CHAIN_DATA_TOGO_LO
21	CHAIN_DATA_TOGO_LO
22	CHAIN_DATA_TOGO_LO
23	CHAIN_DATA_TOGO_LO
24	CHAIN_DATA_TOGO_LO
25	CHAIN_DATA_TOGO_LO
26	CHAIN_DATA_TOGO_LO
27	CHAIN_DATA_TOGO_LO
28	CHAIN_DATA_TOGO_LO
29	CHAIN_DATA_TOGO_LO
30	CHAIN_DATA_TOGO_LO
31	CHAIN_DATA_TOGO_LO

CHAIN_DATA_TOGO_LO RO, CON32[31..0], Alta, Karbon, Neon

This register indicates the low word of the 64-bit number of bytes remaining the DMA chain.

7.7 CON33 Register

Bit	Name
0	CHAIN_DATA_TOGO_HI
1	CHAIN_DATA_TOGO_HI
2	CHAIN_DATA_TOGO_HI
3	CHAIN_DATA_TOGO_HI
4	CHAIN_DATA_TOGO_HI
5	CHAIN_DATA_TOGO_HI
6	CHAIN_DATA_TOGO_HI
7	CHAIN_DATA_TOGO_HI
8	CHAIN_DATA_TOGO_HI
9	CHAIN_DATA_TOGO_HI
10	CHAIN_DATA_TOGO_HI
11	CHAIN_DATA_TOGO_HI
12	CHAIN_DATA_TOGO_HI
13	CHAIN_DATA_TOGO_HI
14	CHAIN_DATA_TOGO_HI
15	CHAIN_DATA_TOGO_HI
16	CHAIN_DATA_TOGO_HI
17	CHAIN_DATA_TOGO_HI
18	CHAIN_DATA_TOGO_HI
19	CHAIN_DATA_TOGO_HI
20	CHAIN_DATA_TOGO_HI
21	CHAIN_DATA_TOGO_HI
22	CHAIN_DATA_TOGO_HI
23	CHAIN_DATA_TOGO_HI
24	CHAIN_DATA_TOGO_HI
25	CHAIN_DATA_TOGO_HI
26	CHAIN_DATA_TOGO_HI
27	CHAIN_DATA_TOGO_HI
28	CHAIN_DATA_TOGO_HI
29	CHAIN_DATA_TOGO_HI
30	CHAIN_DATA_TOGO_HI
31	CHAIN_DATA_TOGO_HI

CHAIN_DATA_TOGO_HI RO, CON33[31..0], Alta, Karbon, Neon

This register indicates the high word of the 64-bit number of bytes remaining the DMA chain.

7.8 CON34 Register

Bit	Name
0	DMA_AUTO_START
1	DMA_ABORT
2	DMA_DIRECTION
3	DMA_DONE
4	DMA_STATUS
5	DMA_STATUS
6	DMA_STATUS
7	DMA_STATUS
8	DMA_NO_RULE
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	DMA_INIT_FUNC
17	DMA_PRIORITY
18	DMA_64_BIT
19	DMA_CHAINING
20	DMA_COMMAND
21	DMA_COMMAND
22	DMA_COMMAND
23	DMA_COMMAND
24	DMA_BEN
25	DMA_BEN
26	DMA_BEN
27	DMA_BEN
28	LATCH_CONTROL
29	LATCH_CONTROL
30	Reserved
31	Reserved

DMA_AUTO_START R/W, CON34[0], Alta, Karbon, Neon

This bit controls how the DMA engine starts.

DMA_AUTO_START	Meaning
0	Do nothing
1	Reload and re-start when CHAIN_DATA_TOGO = 0

DMA_ABORT RO, CON34[1], Alta, Karbon, Neon

This bit immediately aborts DMA. Always reads back 0.

DMA_DIRECTION R/W, CON34[2], Alta, Karbon, Neon

This bit indicates the direction that DMA engine will move data.

DMA_DIRECTION	Meaning
0	DMA write (to host memory)
1	DMA read (from host memory)

DMA_DONE RO, CON34[3], Alta, Karbon, Neon

Future use.

DMA_STATUS RO, CON34[7..4], Alta, Karbon, Neon

Future use.

DMA_NO_RULE R/W, CON34[8], Alta, Karbon, Neon

Setting this bit to a 1 will cause the DMA engine to DMA data as fast as it can. It will not wait for data to be available from the acquisition engine. The actual data that is DMAed will be unpredictable. This bit, therefore, is only useful for diagnostics.

DMA_INIT_FUNC R/W, CON34[16], Alta, Karbon, Neon

Future use.

DMA_PRIORITY R/W, CON34[17], Alta, Karbon, Neon

Future use.

DMA_64_BIT R/W, CON34[18], Alta, Karbon, Neon

Controls where the DMA operations are 64-bit or 32-bit.

DMA_64_BIT	Meaning
0	32-bit DMA operations
1	64-bit DMA operations

DMA_CHAINING RW, CON34[19], Alta, Karbon, Neon

This bit determines whether the DMA engine will execute chaining DMA or not.

DMA_CHAINING	Meaning
0	Execute a single DMA operations
1	Execute a chain of DMA operations

DMA_COMMAND R/W, CON34[23..20], Alta, Karbon, Neon

Controls the DMA engine.

DMA_COMMAND	Meaning
0000b to 1110b	Reserved
1111b	Normal DMA operation

DMA_BEN R/W, CON34[27..24], Alta, Karbon, Neon

Future use.

LATCH_CONTROL R/W, CON34[29..28], Alta, Karbon, Neon

Future use.

7.9 CON35 Register

Bit	Name
0	XFR_PER_INT
1	XFR_PER_INT
2	XFR_PER_INT
3	XFR_PER_INT
4	XFR_PER_INT
5	XFR_PER_INT
6	XFR_PER_INT
7	XFR_PER_INT
8	XFR_PER_INT
9	XFR_PER_INT
10	XFR_PER_INT
11	XFR_PER_INT
12	XFR_PER_INT
13	XFR_PER_INT
14	XFR_PER_INT
15	XFR_PER_INT
16	XFR_PER_INT
17	XFR_PER_INT
18	XFR_PER_INT
19	XFR_PER_INT
20	XFR_PER_INT
21	XFR_PER_INT
22	XFR_PER_INT
23	XFR_PER_INT
24	XFR_PER_INT
25	XFR_PER_INT
26	XFR_PER_INT
27	XFR_PER_INT
28	XFR_PER_INT
29	XFR_PER_INT
30	XFR_PER_INT
31	XFR_PER_INT

XFR_PER_INT R/W, CON35[31..0], Alta, Karbon, Neon

This register controls how often the board issues an EOF interrupt. Every time XFR_PER_INT bytes have been DMAed, the board will emit an interrupt.

7.10 Scatter Gather DMA Instructions

The DMA engine is run by Scatter Gather DMA instructions. These are called “quads” because they generally consist of four words, although the DMA engine only uses three words.. A list of instructions are called a Quad Table or QTAB. Each quad consists of the following entries.

1. Destination address
2. Size of transfer
3. Next quad address.

The following sections document the structure of these quads.

7.11 Destination Address

Bit	Name	Bit	Name
0	Destination Address	32	Destination Address
1	Destination Address	33	Destination Address
2	Destination Address	34	Destination Address
3	Destination Address	35	Destination Address
4	Destination Address	36	Destination Address
5	Destination Address	37	Destination Address
6	Destination Address	38	Destination Address
7	Destination Address	39	Destination Address
8	Destination Address	40	Destination Address
9	Destination Address	41	Destination Address
10	Destination Address	42	Destination Address
11	Destination Address	43	Destination Address
12	Destination Address	44	Destination Address
13	Destination Address	45	Destination Address
14	Destination Address	46	Destination Address
15	Destination Address	47	Destination Address
16	Destination Address	48	Destination Address
17	Destination Address	49	Destination Address
18	Destination Address	50	Destination Address
19	Destination Address	51	Destination Address
20	Destination Address	52	Destination Address
21	Destination Address	53	Destination Address
22	Destination Address	54	Destination Address
23	Destination Address	55	Destination Address
24	Destination Address	56	Destination Address
25	Destination Address	57	Destination Address
26	Destination Address	58	Destination Address
27	Destination Address	59	Destination Address
28	Destination Address	60	Destination Address
29	Destination Address	61	Destination Address
30	Destination Address	62	Destination Address
31	Destination Address	63	Destination Address

7.12 Size of Transfer

Bit	Name
0	Data Size
1	Data Size
2	Data Size
3	Data Size
4	Data Size
5	Data Size
6	Data Size
7	Data Size
8	Data Size
9	Data Size
10	Data Size
11	Data Size
12	Data Size
13	Data Size
14	Data Size
15	Data Size
16	Data Size
17	Data Size
18	Data Size
19	Data Size
20	Data Size
21	Data Size
22	Data Size
23	Data Size
24	Data Size
25	Data Size
26	Data Size
27	Data Size
28	Data Size
29	Data Size
30	Data Size
31	Data Size

7.13 Next Quad Address

Bit	Name	Bit	Name
0	Next Quad Address	32	Next Quad Address
1	Next Quad Address	33	Next Quad Address
2	Next Quad Address	34	Next Quad Address
3	Next Quad Address	35	Next Quad Address
4	Next Quad Address	36	Next Quad Address
5	Next Quad Address	37	Next Quad Address
6	Next Quad Address	38	Next Quad Address
7	Next Quad Address	39	Next Quad Address
8	Next Quad Address	40	Next Quad Address
9	Next Quad Address	41	Next Quad Address
10	Next Quad Address	42	Next Quad Address
11	Next Quad Address	43	Next Quad Address
12	Next Quad Address	44	Next Quad Address
13	Next Quad Address	45	Next Quad Address
14	Next Quad Address	46	Next Quad Address
15	Next Quad Address	47	Next Quad Address
16	Next Quad Address	48	Next Quad Address
17	Next Quad Address	49	Next Quad Address
18	Next Quad Address	50	Next Quad Address
19	Next Quad Address	51	Next Quad Address
20	Next Quad Address	52	Next Quad Address
21	Next Quad Address	53	Next Quad Address
22	Next Quad Address	54	Next Quad Address
23	Next Quad Address	55	Next Quad Address
24	Next Quad Address	56	Next Quad Address
25	Next Quad Address	57	Next Quad Address
26	Next Quad Address	58	Next Quad Address
27	Next Quad Address	59	Next Quad Address
28	Next Quad Address	60	Next Quad Address
29	Next Quad Address	61	Next Quad Address
30	Next Quad Address	62	Next Quad Address
31	Next Quad Address	63	Next Quad Address

Register and Memory Mapping

Chapter 8

8.1 Introduction

This section explains how the registers and the various chunks of memory are mapped and accessed on the Alta/Karbon/Neon and their virtual frame grabbers.

8.2 Memory Types

8.2.1 Registers

All registers are 64 bits wide and on 64-bit boundary. With the exception of the DPM, only data bits 31 to 0 are used, bits 63 to 32 are always “don't care”. The DPM uses all 64 bits. Out of the lower 32 LSBs, some registers use only a portion of the bits. Registers can also be accessed as 32 bit wide. Little endian addressing is used, i.e. MSB is bits 63-56.

8.2.2 UART

The UART is 8 bit wide and its registers are on 64-bit boundary. The UART is only on the Karbon and Neon.

8.2.3 DPM

The DPM is 64 bit wide. The DPM can be accessed as 64-bit (on 64-bit boundary) or as 32-bit wide (on 32-bit boundary) memory. During acquisition (GRAB/SNAP), the slave read from DPM is inhibited. In this case, data read will be always zero.

Note: The DPM is only accessible form host on the R64.

8.2.4 CTABs

The CTabs for the Karbon, Alta and Neon are implemented slightly differently than the R64. These CTabs are Run Length Encoded (RLE). The RLE CTabs are stored in the same address space as is used for the CTabs on the R64, however, only the first 256 locations are actually populated. This reason this works is that the RLE CTabs can compress the normal CTabs by a very large amount, considerably reduce that memory requirements for CTabs.

8.3 Memory Map

The following table illustrates the physical location of the various sections of memory on the board. The addresses are offset from the BAR1 PCI base address..

Memory	Address (hex)	Comment
CON0	00 80 00 00	download, clock control
CON1	00 00 00 00	Camera Control Register
CON2	00 02 00 00	Camera Control Register
CON3	00 04 00 00	Camera Control Register
CON4	00 06 00 00	Camera Control Register
CON5	00 08 00 00	Camera Control Register
CON6	00 0A 00 00	Camera Control Register
CON7	00 0C 00 00	Camera Control Register
CON8	00 0E 00 00	Camera Control Register
CON9	00 10 00 00	Camera Control Register
CON10	00 10 00 08	Camera Control Register
CON11	00 10 00 10	Camera Control Register
CON12	00 10 00 18	Camera Control Register
CON13	00 10 00 20	Camera Control Register
CON14	00 10 00 28	Camera Control Register
CON15	00 00 00 08	Camera Control Register
CON16	00 00 00 10	Camera Control Register
CON17	00 00 00 18	Camera Control Register
CON18	00 00 00 20	Camera Control Register
CON19	00 00 00 28	Camera Control Register
CON20	00 10 00 30	Camera Control Register
CON21	00 10 00 38	Camera Control Register
CON22	00 00 00 30	Camera Control Register
CON23	00 00 00 38	Camera Control Register
CON24	00 10 00 40	Camera Control Register
CON25	00 10 00 48	Camera Control Register
CON26	00 00 00 40	Camera Control Register
CON27	00 00 00 48	Camera Control Register
CON28	00 00 00 50	DMA Register
CON29	00 00 00 58	DMA Register
CON30	00 00 00 60	DMA Register
CON31	00 00 00 68	DMA Register
CON32	00 00 00 70	DMA Register
CON33	00 00 00 78	DMA Register
CON34	00 00 00 80	DMA Register
CON35	00 00 00 88	DMA Register
CON36	00 80 00 18	Alta/Neon Only
CON37	00 80 00 20	Alta/Neon Only
CON38	00 80 00 28	Neon Only
CON40	00 00 00 98	Alta Only

Memory	Address (hex)	Comment
CON41	00 00 00 A0	Alta Only
CON42	00 00 00 A8	Alta Only
CON43	00 00 00 B0	Alta Only
CON44	00 00 00 B8	Alta Only
CON45	00 00 00 C0	Alta Only
CON46	00 00 00 C8	Alta Only
CON47	00 00 00 D0	Alta Only
CON48	00 00 00 D8	Alta Only
CON49	00 00 00 E0	Alta Only
CON50	00 00 00 E8	Alta Only
CON51	00 00 00 F0	Camera Control Register
CTABS	00 20 00 00	Only first 256 address populated
DPM	00 50 00 00	Dual ported memory, R64 Only
UART	00 70 00 00	8 internal 8-bit registers on 64 bit boundary, Karbon/None only
RO_INFOHI	00 80 00 08	R/O info, model/rev, etc.
RO_INFOLO	00 80 00 10	R/O info, model/rev, etc.

The following pertains to the table above.

All registers are treated as 64 bits wide.
Two BARs are allocated for PCI access.
BAR0, is not currently used.
BAR1, memory mapped, 16M size, is used for access to registers, CTABs, DPM.

8.4 Downloading Firmware

On the Karbon family, firmware is downloaded using a special downloader module. The downloader module always resident on the board. When flashing the FPGA, either the download module can be written or the real firmware (written to the board from the host) can be written to the chip.

On the Alta and Neon families, download is facilitated by writing to board resident SRAM. This SRAM is always available on the board and is access indirectly. Once the SRAM is loaded with new firmware, the board's FPGAs can be flashed directly from the SRAM.

8.5 PCI Configuration Space and Model/Revision Information

Each family of boards has its own device ID as follows:

Alta - 0x5000
Karbon - 0x3000
Neon - 0x4000

Information about different models and board capabilities is stored in the INFO_HI and INFO_LO registers.

Specifications

Chapter 9

9.1 Introduction

This chapter describes the general specifications of the Alta family. The numerical values for he specifications are listed in Table 9-1. If more information is available for a given specification there will be an entry in the column marked “Details”.

Table 9-1 Alta-AN Specifications

Specifications	Value	Units	Details
PCIe Compatibility	x4, x8 and x16	Slot size	
Temperature range	0 to 50	Degrees Celsius	
Humidity	25% to 80%		
Mechanical dimensions	6.8 x 4.2	Inches	
Mechanical dimensions	17.4 x 10.6	Centimeters	
Digitizer bits per channel	8	Bits	
Maximum channels per VFG	3		
Maximum A/D conversion frequency	100 MHz	MHz	
Analog input voltage range	0.35 to 1.4	Volts P-to-P	
Gain adjustment range	±6	dB	
Gain adjustment resolution	8	Bits	
Gain matching between channels	±1%	of full scale	
Offset adjustment range	±127	LSB	
Maximum frame size	16K x 16K	Pixels	
Power for camera	12	Volts @ 0.5 Amps	
Differential non-linearity typical	±0.5	LSB	
Differential non-linearity maximum	+1.0/-0.9	LSB	
Integral non-linearity typical	±1.1	LSB	

Table 9-1 Alta-AN Specifications

Specifications	Value	Units	Details
Integral non-linearity maximum	±2.75	LSB	
PLL jitter typical	250	picoseconds P-to-P	
PLL jitter maximum	450	picoseconds P-to-P	
HSYNC Frequency Range	10 to 150	kHz	

Mechanical

Chapter 10

10.1 Introduction

This chapter describes the mechanical characteristics of the Alta analog frame grabber. This includes description of all of the connectors on the board and pin-outs for these connectors.

The Alta-AN is available in three version. The ALT-PCE-AN1, which supports one camera (with up to three taps), the ALT-PCE-AN2, which supports two independent cameras (with up to three taps each) and the ALT-PCE-AN4, which supports up to four independent cameras (with up to three taps each). All three versions use the same basic laminate. The three models just have different parts populated.

The mechanical layout of the ALta-AN main board is shown in Figure 10-1.

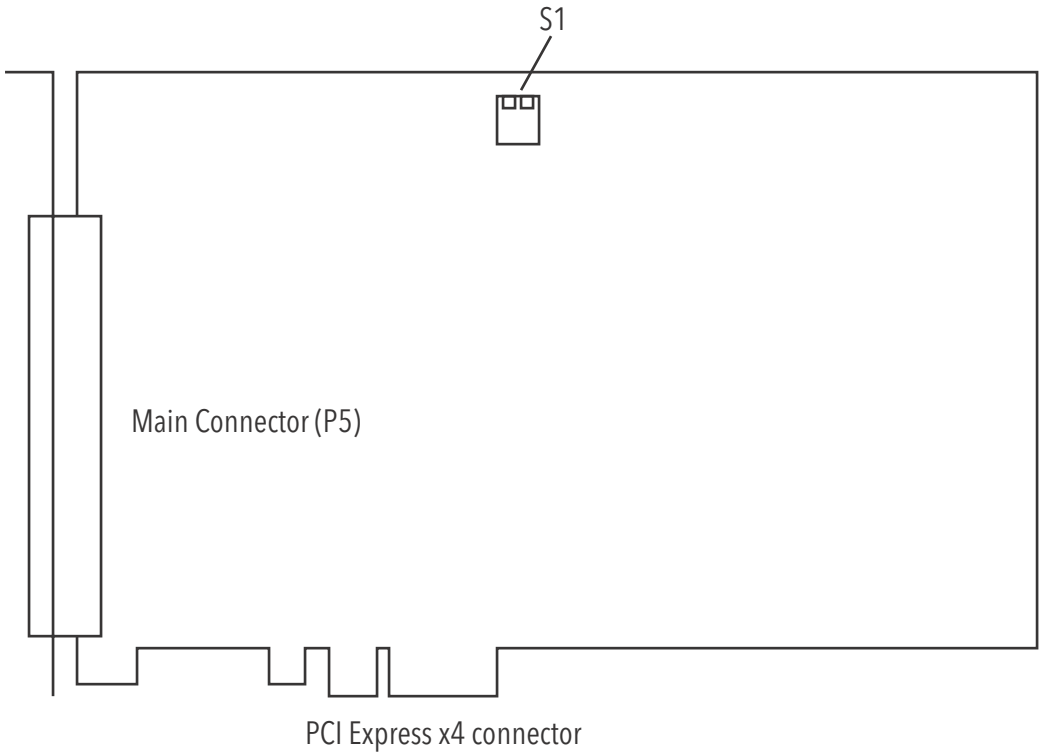

Figure 10-1 Alta-AN Main Board Layout

10.2 The Alta-AN Connector (P5)

The Atla-AN has only one main connector. This connector provides access to all of the video inputs, as well as synchronization inputs and outputs. Power is also provided. Table 10-1shows the pinout.

The connector is a 62-pin female, three-row, D Sub connector. A variety of cables are available from BitFlow, as well as a mating connector kit.

Note: The pinout below shows all of the possible connections on the Alta-AN. The ALT-PCE-AN4 model has all of these connections. However, the ALT-PCE-AN2 only has the connections marked VFG0 and VFG1. Similarly, the ALT-PCE-AN1 only has the connections marked VFG0

Note: All non-video signals, both in and out of the board, at 3 Volt TTL signals.

Note: The 12 Volt power is intended to power cameras only. The camera must not draw more than 0.5 Amps.

Note: Connect 1-tap cameras to the VIDEO1 port on each VFG. Connect 2-tap cameras to the VIDEO0 and VIDEO1 ports on each VFG. For color cameras, connect R, G and B to VIDEO0, VIDEO1 and VIDEO2 ports respectively.

.

Table 10-1 Alta-AN Main Connector

Pin	In/Out	Signal	1-tap Cameras	2-tap Cameras	Color Cameras
1	IN	VFG0_VIDEO2			Cam0, B
2	IN	VFG0_VIDEO1	Cam0	Cam0,Tap1	Cam0, G
3		AGND			
4		AGND			
5	Power	VFG0_12V_POWER			
6		AGND			
7	Power	VFG1_12V_POWER			
8	IN	VFG1_VIDEO3			
9	IN	VFG1_VIDEO1	Cam1	Cam1, Tap1	Cam1, G
10	IN	VFG1_VIDEO0		Cam1, Tap0	Cam1, R
11		AGND			
12		AGND			
13	Power	VFG2_12V_POWER			
14		AGND			
15	IN	VFG2_VIDEO3			
16	IN	VFG2_VIDEO1	Cam2	Cam2, Tap1	Cam2, G
17		AGND			
18		AGND			
19	Power	VFG3_12V_POWER			
20	IN	VFG3_VIDEO3			
21	IN	VFG3_VIDEO2			Cam3, B

Table 10-1 Alta-AN Main Connector

Pin	In/Out	Signal	1-tap Cameras	2-tap Cameras	Color Cameras
22	IN	VFG0_VIDEO3			
23	IN	VFG0_VIDEO0		Cam0, Tap0	Cam0, R
24	IN/OUT	VFG0_HD			
25	OUT	VFG0_TRIGGER_OUT			
26	IN	VFG0_WEN			
27	OUT	VFG1_TRIGGER_OUT			
28	IN/OUT	VFG1_VD			
29	IN/OUT	VFG1_HD			
30	IN	VFG1_VIDEO2			Cam1, B
31	IN	VFG3_WEN			
32	IN	VFG1_WEN			
33	IN	VFG2_TRIGGER_IN			
34	OUT	VFG2_STROBE			
35	IN/OUT	VFG2_VD			
36	IN	VFG2_VIDEO2			Cam2, B
37	IN	VFG2_VIDEO0		Cam2, Tap0	Cam2, R
38	IN/OUT	VFG3_VD			
39	OUT	VFG3_TRIGGER_OUT			
40	OUT	VFG3_STROBE			
41	IN	VFG3_VIDEO1	Cam3	Cam3, Tap1	Cam3, G
42	IN	VFG3_VIDEO0		Cam3, Tap0	Cam3, R
43		GND			
44		GND			
45	IN	VFG0_TRIGGER_IN			
46	OUT	VFG0_STROBE			
47	IN/OUT	VFG0_VD			
48		GND			
49		GND			
50	IN	VFG1_TRIGGER_IN			
51	OUT	VFG1_STROBE			
52		GND			
53		GND			
54		GND			
55	IN/OUT	VFG2_HD			
56	OUT	VFG2_TRIGGER_OUT			
57	IN	VFG2_WEN			
58		GND			
59		GND			
60	IN/OUT	VFG3_HD			
61	IN	VFG3_TRIGGER_IN			
62		GND			

10.3 Switches

There is one piano-type switch block, S1, on the Alta-AN with two switches. These are used to identify individual boards when there is more than one board in a system. The idea is to set the switches differently on each board in the system. The switch settings can be read for each board from software (by reading the SW bitfield). SysReg also shows the switch setting for each board. See Table 10-2 below shows the switch settings and the corresponding value in the SW bitfield.

Table 10-2 Switch S1 Setting

S1.1	S1.2	SW register
down	down	0
down	up	1
up	down	2
up	up	3

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